Capacitance Measurements of Single Indium Arsenide Nanowires

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Abstract and Introduction:

Recently, semiconductor nanowires have been given much attention as potential candidates for future high-end electronic devices due to their one-dimensional transport and favorable geometry for processing all-around gates with improved electrostatics. As for the material for the nanowire, of particular interest is indium arsenide (InAs), which has a very high bulk mobility at room temperature. However to date, very little experimental evidence is available on the mobility of single InAs nanowires due to the difficulty of obtaining accurate gate capacitance measurements over parasitics which can be orders of magnitudes higher. In this project, InAs nanowire field effect transistors (FETs) were fabricated and capacitance-voltage (C-V) measurements were carried out using a calibration setup involving open and short circuits to calibrate out any parasitic elements.

Experimental Procedure:

Electron beam lithography (EBL) was used to define contact pads and scanning electron microscopy (SEM) markers (Figure 1) on *p*-type silicon wafers with 200 nm of thermally grown silicon dioxide (SiO_2). The contact pads were designed as 60 × 60 μm squares with 40 μm spacing to be compatible with RF measurement probes which were used to conduct the capacitance measurements.

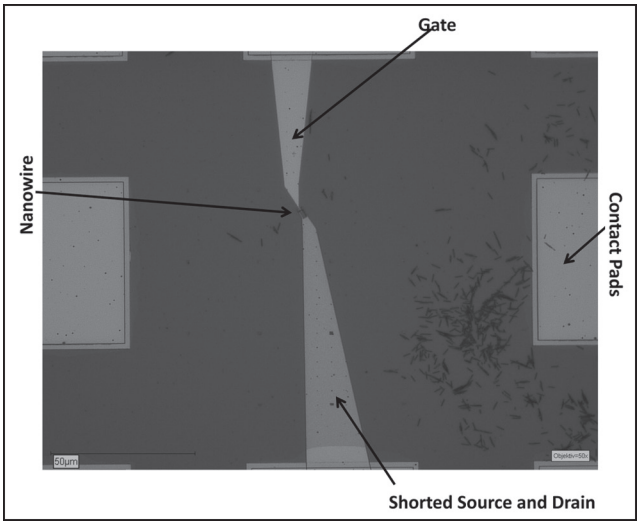

Figure 1: Optical image of a device for capacitance measurements.

InAs nanowires grown by molecular beam epitaxy (MBE) were transferred onto the samples using a mechanical transfer method. The wires, characterized beforehand, had an average length and diameter of 1.9 μm and 93 nm respectively. SEM images of each field with markers were taken to locate the position of the nanowires. Contacts to the wires were subsequently designed in Autocad using the SEM images.

Three different types of devices were designed and processed so that different types of measurements could be carried. Four terminal devices were fabricated for four point probe measurements to extract the resistivity of the wires. Three terminal FET devices with a top gate were fabricated so that transistor measurements could be carried out. Also, two terminal devices with a top gate and shorted source and drain contacts were designed for capacitance measurements. Regarding the devices fabricated for capacitance measurements, two more fields with identical contact structures—one with a short between the source, drain and gate contacts in place of the nanowire and one with an open circuit—were also fabricated for calibration purposes. The capacitance of the open circuit is measured to calibrate out the parasitic capacitances while the short circuit is used to account for any parasitic inductances.

The source-drain contacts were defined using EBL and after metal deposition, 50 nm of lanthanum lutetium oxide ($LaLuO_3$) with a dielectric constant of 20 was deposited as a high-κ gate dielectric onto the samples using pulsed laser deposition (PLD). The gate contacts were then processed using EBL. Finally, using EBL again, the $LaLuO_3$, on top of the contact pads, was etched by a buffered hydrochloric acid/ammonia solution so measurement probes could contact the pad metal.

Results and Conclusions:

Four-point-probe resistivity measurements were carried out on nanowire devices with inner contact spacings of approximately 600 nm. Resistances ranging between

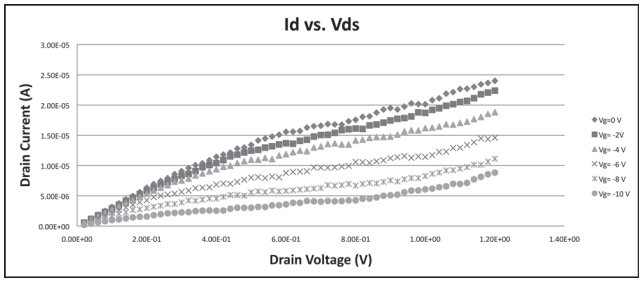

Figure 2: Drain current vs. drain voltage graph for different gate voltages.

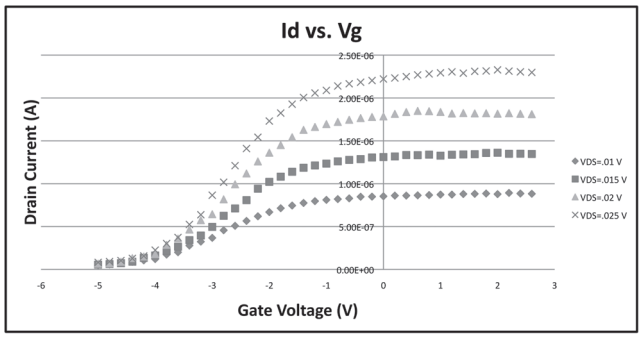

Figure 3: Drain current vs. gate voltage graph for different drain voltages.

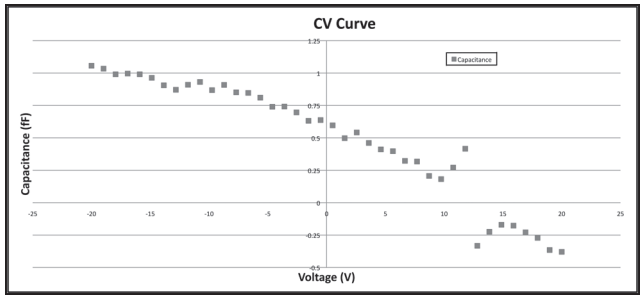

Figure 4: Capacitance-voltage characteristics obtained with an AC signal of 500 mV at 45 MHz.

4-20 kΩ were measured, resulting in resistivities between 4.5-23 mΩ-cm. Two point probe resistance measurements were also carried out to determine the contact resistances of the devices. Measuring resistance values between contacts of different spacings, and extrapolating down to a spacing of 0.0 nm, yielded contact resistances in the 1 kΩ range, indicating good ohmic contacts.

For the transistor measurements, sweeps of both source-drain and gate voltages were conducted to obtain characteristic curves (Figure 2) and the transfer characteristics of the nanowire FETs (Figure 3). The measured device had a gate length of 160 nm and source-drain distance of 2.25 μm. From the transfer characteristics graph, we found the transconductance of the device, calculated as $g_m = dI_d/dV_g$, to be 1.14 μS at a source-drain bias of 25 mV.

Capacitance measurements were carried out with an Agilent 4294A Precision Impedance Analyzer using RF probe tips at a frequency of 45 MHz with a 500 mV signal [1]. From Figure 4, it can be seen that the measured capacitance with no applied bias is 620 aF. The field effect mobility is calculated as [2]

$$\mu_{FE} = \frac{g_m L_G^2}{C V_{DS}}$$

where L_G is the gate length, C is the gate capacitance and V_{DS} is the applied source-drain voltage. Using the data from the transistor measurements, this yields a field effect mobility of 188 $cm^2V^{-1}s^{-1}$. We were unable to obtain a full CV curve because as can be seen in the figure, the device breaks down at around 10 V bias.

The theoretical gate capacitance of the wires is calculated as [2]

$$C = \frac{2\pi\epsilon L_G}{\ln\left[\left(t_{ox} + r + \sqrt{(t_{ox}+r)^2 - r^2}\right)/r\right]}$$

where t_{ox} is the oxide thickness and r is the nanowire radius. This leads to a theoretical capacitance of 131 aF, which is much lower than the capacitance measured. This large difference can be partly attributed to a fabrication error for the shorted calibration devices which required manually fabricating a short with a bonded wire, decreasing the accuracy of the measurement.

Future Work:

Through this project, we have successfully fabricated nanowire FETs using MBE grown InAs nanowires and shown the possibility of obtaining the capacitances of individual nanowires. However, more work must be done to ensure that the measurements are more accurate and future work will include fabricating devices with working short calibrations and possibly doing capacitance measurements in a low temperature environment.

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References:

[1] "The Parametric Measurement Handbook"; Agilent Tech. (2010).

[2] Dayeh, S., et al.; "High Electron Mobility InAs Nanowire Field-Effect Transistors"; Small, 3, 326-332 (2007).