

Characterization of Silicon Oxide Etching with Low Global Warming Potential Hydroolefin

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Primary CNF Tools Used: Gamma Automatic Coat-Develop Tool, ASML PAS 5500/300C DUV Wafer Stepper, P7 Profilometer, Zeiss Ultra SEM, Zeiss Supra SEM, Oxford 82 Etcher, Oxford 100 ICP-RIE Dielectric Etcher, YES EcoClean Asher, and Thermal Oxidation Furnace

Abstract:

The semiconductor industry utilizes hydrofluorocarbons (HFCs) for many different etch processes. HFCs, however, have high global warming potential (GWP). The American Innovation and Manufacturing Act of 2020 enabled the U.S. EPA to scale down the use and production of HFCs. Hydroolefins (HFOs), originally created by the refrigerant industry to reduce reliance on HFCs, show promise as an etch gas in reactively ion etched (RIE) anisotropic etching. This work explores the optimal etch conditions of

HFO-1234ze(E), or $C_3H_2F_4$ on the Oxford PlasmaLab 100 Inductively Coupled Plasma Reactive Ion Etcher. Etch rates remained similar to other oxide etch chemistries, though RIE lag remains a concern, especially with higher concentrations of $C_3H_2F_4$ in the plasma. Deposition and delamination occurred occasionally in the process of characterization, when $C_3H_2F_4$ concentration was too high or the DC voltage bias became too low. $C_3H_2F_4$ holds promise for regular use as a silicon oxide etch gas with more characterization and process research.

Summary of Research:

Silicon oxide is a common etch material in the semiconductor industry and is often etched with hydrofluorocarbons (HFCs) for their versatility and availability¹. Though HFCs are not ozone-depleting, they have high global warming potentials (GWP), contributing to global warming in the atmosphere. The AIM Act of 2020 allowed the EPA to begin the scale down in use and production of HFCs, creating a need in the semiconductor industry for new silicon oxide etch gases. HFO-1234ze(E), or $C_3H_2F_4$ has shown potential in silicon etching but it has not been characterized definitively^{1,2}. A broad analysis was thus conducted to test the etch rate, selectivity, sidewall angle, and RIElag

of various etch recipes of $C_3H_2F_4$. RIElag is the effect of smaller features etching at a slower rate to larger features. It can be reduced by altering the properties of an etch plasma. The Oxford PlasmaLab 100 was used to characterize $C_3H_2F_4$ since, as an ICP etcher, it allowed the individual control of multiple different parameters, controlling the plasma both chemically and physically. Patterned and blank silicon oxide wafers were tested on the Oxford 100 over the course of the experiments.

About 1 micron of silicon oxide grown on Silicon test wafers in a wet oxide furnace. Most wafers were patterned using the Gamma Automatic Coat-Develop Tool, though some wafers were hand-spun, replicating the Gamma processes. BARC was spun on wafers for 30 seconds at 2400 rpm, before a 60-second, 205° bake. Next, UV210-0.6 photoresist was spun at 2900 rpm for 30 seconds, with a 60-second, 135° bake. The wafers were patterned using the ASML PAS 5500/300C DUV Wafer Stepper. Two patterns were used, a standard edge-clear pattern and the ALE Test Mask for RIElag that has trenches of varying width, from 5 micron to 300 nm, with large additional corner features. Finally, the wafers were developed with a 135° bake for 90 seconds, before a 60-second 724MIF develop.

Every patterned wafer had an BARC removal with a I-minute, 45-second ARC etch on the Oxford 82. After, step height of the large corner features was measured with the P7 Profilometer using a shortened version of a pre-existing sequence, testing 10 different corners. Each wafer was etched in the Oxford 100. Prior to each etch, the Oxford 100 was cleaned and seasoned for 2 minutes with either a bare silicon wafer or a blank silicon oxide wafer, to test for deposition. After etching in the Oxford 100, the P7 sequence was run again before the wafer was cleaned with a 5-minute photoresist-strip recipe on the YES EcoClean Asher. A last step height measurement was taken with the P7 sequence. Each relevant wafer's

depth and sidewall angle of the largest and smallest feature was measured using the Zeiss SEM Ultra. Wafers with deposition etches were measured for the height of the deposition. Wafers that delaminated or etched less than 40 nm of silicon oxide were not measured on the SEM.

Table 1: Initial Characterization Etches and Results.

Etch Recipe and Time	Oxide Etch Rate (nm/min)	Selectivity Oxide:Resist	Avg. Sidewall Angle	RIELAG
C ₃ H ₂ F ₄ High He (2 min)	217	6.3	95	0.72
CH ₂ F ₂ /High He (116 sec)	156	2.8	98	0.80
CHF ₃ /O ₂ Oxide (2 min)	168	1.7	93	0.83
C ₃ F ₈ /High He Oxide (2 min)	261	1.4	135	0.98
5 sccm CH ₂ F ₂ , 40 sccm C ₃ F ₈ , 3 sccm C ₃ F ₆ , 20 sccm Ar (2 min)	231	1.9	127	0.98

Table 2: Final Experiment Parameters

Parameter	Min	Max
ICP (W)	1500	2500
RIE (W)	40	80
Pressure mTorr	4	8
Gas Ring	Off	On
C ₃ H ₂ F ₄ (sccm)	10	30
He (sccm)	20	90
Ar (sccm)	0	50

Table 1 (Left): The five etches used and their resulting etch rates.

Table 2 (Right): Final Experiment Parameters.

A round of characterization etches compared the capabilities of the given C₃H₂F₄ recipe to that of other common silicon oxide etch recipes. Table 1 shows the five etches used and their resulting etch rate, selectivity, and RIElag. RIElag was calculated by the ratio of the smallest feature's depth to the largest feature's depth; the closer the value to 1, the less lag in etch rate of smaller features. The results confirmed that C₃H₂F₄ held potential as a silicon oxide etch gas. It had similar results in etch rate and sidewall angle, which was measured as the inside angle from the etched depth to the sidewall. Selectivity was improved from the other etches, but RIElag was worse. Thus, RIElag was the focused goal of continuing experimentation with additional goals of staying on target with selectivity, etch rates, and sidewall angle.

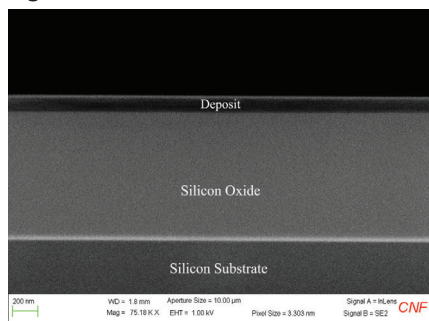


Figure 1: Deposition wafer.

Next, an experiment was designed using the JMP DOE software to find the optimal way to characterize multiple parameters within the etch recipe in a minimum number of wafers. The initial parameters used were the chamber pressure, the RF power, the ICP power, the usage of the gas ring to dispense C₃H₂F₄, and the concentration of C₃H₂F₄ to Helium. The experiment, however, immediately resulted in much deposition instead of etching. The experiment was ended to allow for more characterization attempts with blank silicon

oxide wafers to determine better value ranges for each parameter. Many of these characterization attempts resulted in deposition, with some wafers having nearly 400 nm of C₂F₄ deposited in 2 minutes, and delamination, slowly approaching more appropriate value ranges. A deposition wafer is shown in Figure 1. From this characterization, it was determined that high concentrations of C₃H₂F₄ and low DC voltage bias were likely causes of deposition.

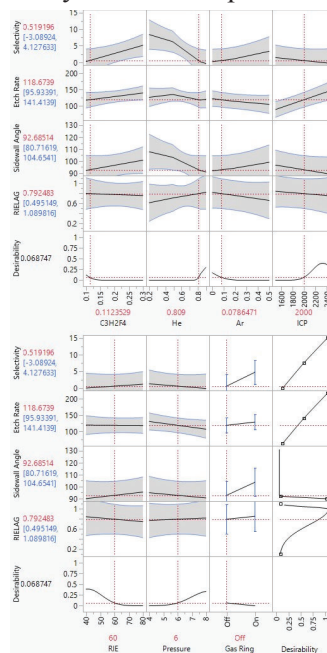


Figure 2: Results from Argon addition.

target with other silicon oxide etch recipes. RIElag varied with only a few recipes improving from the original's capability. From the results, it is evidenced that lower concentrations of C₃H₂F₄ with higher concentrations of Helium result in the best etch rate, RIElag, and sidewall angle. It should also be noted that there is a connection between increased RIE power and decreased RIElag, which would be a site for future research to build on. Though the results of this study were broad, they support further research and characterization on C₃H₂F₄ for future use across the semiconductor industry as a low GWP silicon oxide etch gas.

References:

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