Metal-Oxide Interface Preservation Using Atomic Layer Deposited Metal Interlayers

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Abstract:

Energetic metal deposition techniques have been shown to introduce defects at the metal–oxide (MO) interface, degrading the electrical performance of gate dielectrics in MOS structures. In this work, we compare MO interface degradation resulting from conventional energetic metallization techniques with that of atomic layer deposited (ALD) gate metals. We demonstrate that fully in-situ ALD dielectric and metal deposition provides minimal improvement over post-passivation ALD metallization, indicating that air exposure following ALD passivation does not significantly degrade interface quality. Finally, we show that thin ALD gate metals preserve the MO interface during subsequent energetic metal deposition, enabling additional metallization without measurable degradation of dielectric performance. These results demonstrate that thin ALD metal interlayers provide an effective strategy for preserving MO interface quality while maintaining flexibility in subsequent metallization processes and material selection.

Summary of Research:

Energetic Physical Vapor Deposition (PVD) gate metallizations have been shown to degrade dielectric quality through the introduction of defect states [1]. X-Ray and UV radiation from Magnetron Sputtering and Electron-Beam Evaporation (EBE) can break dielectric bonds. Argon ions from Sputter plasma embed themselves deep in the dielectric [1]. According to the Multiphonon Trap Assisted Tunnelling (TAT) theory, Fowler-Nordheim (FN) TAT is maximized when defect states lie 29.3% of the tunnelling barrier distance away from the cathode (x*) [2], [3]. Interface trap states can also increase TAT by lowering the effective barrier at the Metal-Oxide (MO) interface (ΦMO) as seen in Fig. 1. Higher initial tunnelling current (I0) results in earlier time-to-breakdown (tBD) due to a higher population of lucky electrons as shown in Fig. 2 [2]. This means that the more penetrative the deposition is, the faster the device will break.

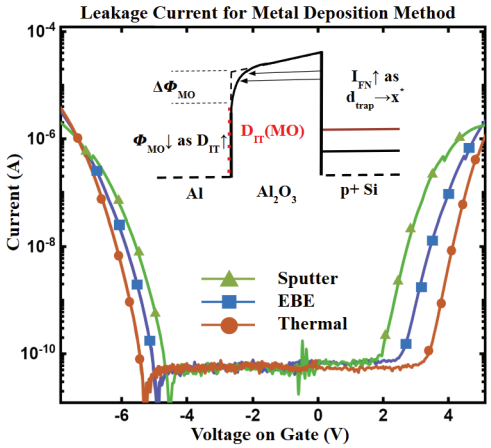

Figure 1: I-V sweeps on 180 μm DIA pads on 15 nm Al_2O_3. Traps at the MO interface lower the effective barrier ΦMO. Sputtering results in the earliest onset current due to high DIT (- bias) and deep dtrap (+ bias).

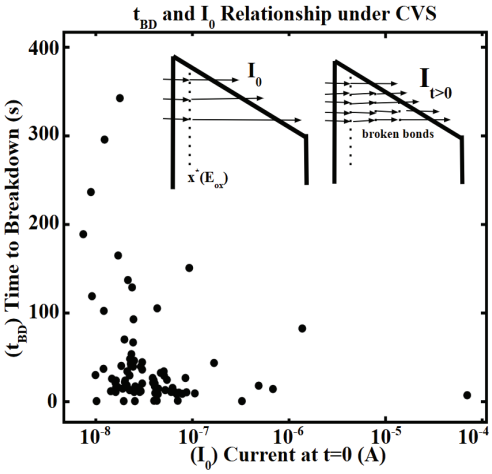

Figure 2: Time-to-breakdown is plotted against initial leakage current at constant voltage stress (CVS). It is shown that higher tBD is achieved when I0 is low. High defect density at x results in maximized I0.*

We fabricate nine Al/Al_2O_3/p+Si MOS capacitors with varied metallization methods. C-V measurements show oxide capacitance (Cox) remains comparable between the samples, indicating Al_2O_3 thickness and dielectric constant (εox) are unchanged. In Fig. 1 our I-V plot confirms literature reports that Sputtering results in the earliest onset TAT, followed by EBE and Thermal Evaporation [1]. Positive bias likely represents increased FN current due to barrier lowering, while negative bias likely indicates trap-limited Frenkel-Poole (FP) tunnelling. Three Thermally Evaporated samples are produced with 30, 15, and 5 nm oxides to access thickness dependence. C-V measurements confirm a plausible Density of Interface Traps (DIT) and Cox thickness trend, J-E leakage plots showed no dependence on thickness, further indicating that leakage through the Al_2O_3 is largely governed by interfacial defects.

After the energetic PVD study we fabricate TiNx/Al_2O_3/p+Si MOS capacitors with ALD metallization. J-E plots showed almost 2x increase in negative bias TAT onset field for ALD metallization compared to Thermal. The 0.5 eV increase in ΦMO from Al to TiNx is not relevant to our J-E negative sweeps which are largely dominated by trap-limited FP tunnelling. FN tunnelling still occurs, but the tunnelling barrier is too thick for ΦMO to be rate-limiting. Time-dependent dielectric breakdown (TDDB) measurements under constant voltage stress (CVS) in Fig. 3 confirm that ALD metallization yields higher tBD when compared to Thermal. This likely arises from the significantly lower leakage current I0 in the ALD sample [2].

Despite its proven advantages, the cost, processing time, and material limitations of ALD have hindered its widespread adoption as a gate metallization technique. We demonstrate that integrating a thin ALD metallization layer between dielectric deposition and conventional PVD metallization enables broader process compatibility while preserving MO interface integrity. We compare EBE Cr (150nm) deposited on TiNx (40 nm) and Al_2O_3 (7 nm) ALD films grown under vacuum with an identical film that was exposed to atmosphere between Al_2O_3 and TiNx. We additionally compare a vacuum-deposited TiNx/Al_2O_3 film with no EBE Cr. Weibull analysis in Fig. 4 reveals no variation in tBD or Weibull slope (β) between the three samples. Additionally, negative field J-E sweeps appear consistent across samples. From this analysis we can infer that the MO interface is protected from EBE by 40 nm TiNx and oxygen defects at the MO surface have little impact on tunnelling current. This follows our earlier framework, as oxygen defects are significantly shallower than x* [3].

In this work we demonstrate dielectric quality degradation across various energetic PVD methods [1] and compare an example of ALD metallization. We have shown that 40 nm TiNx can be deposited on Al_2O_3 after air-transfer and prior to EBE of Cr while still preserving the metal-oxide interface. This work establishes the foundation for ALD interlayer engineering. Future studies should determine the minimum effective interlayer thickness and evaluate compatibility with a broader range of metallization schemes, ultimately enabling a universal metal–oxide interface protection layer.

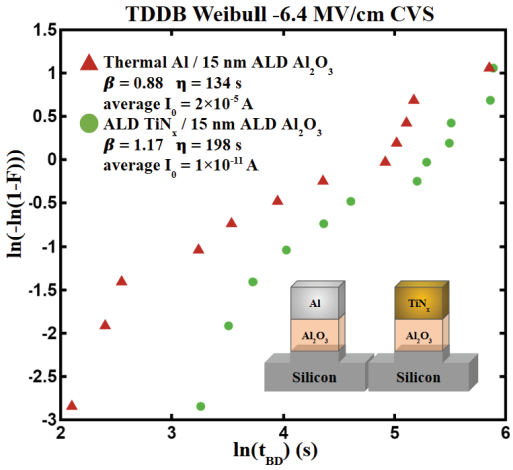

Figure 3: TDDB under CVS at -6.4MV/cm (~90% of EBD). Weibull slope (β) was poor but comparable between samples. The intrinsic time-to-breakdown lifetime (η) increased 47% from Thermal to ALD, while early breakdown times increased almost 177%. We observe 6 orders of magnitude decrease in current at t = 0 from Thermal to ALD.

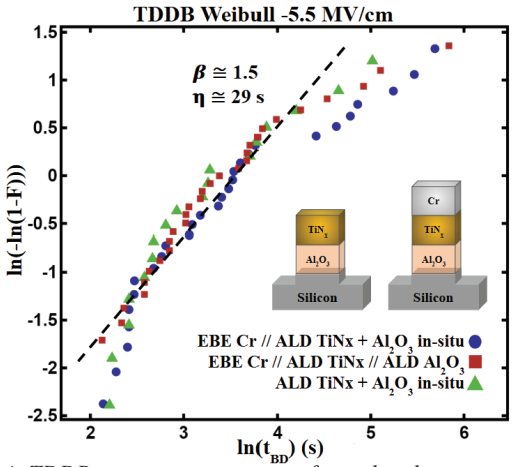

Figure 4: TDDB measurements are performed under constant voltage stress (CVS) at -5.5MV/cm (~90% of EBD). Weibull slope (β) and intrinsic time-to-breakdown lifetime (η) remain consistent across each sample. No change in leakage I0 was observed.

References:

[1] I. Mack et al., "Quantifying the Impact of Al Deposition Method on Underlying Al2O3/Si Interface Quality," Phys. Status Solidi.

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[3] S. Makram-Ebeid and M. Lannoo, "Quantum Model for Phonon-Assisted Tunnel Ionization of Deep Levels in a Semiconductor," Phys. Rev.