Silicon Interposer for Millimeter-Wave Heterogeneous Integration: Doped vs High Resistivity Substrates

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Primary CNF Tools Used: SUSS MA6-BA6 Contact Aligner, AJA Sputter Deposition, UNAXIS 770 Deep Silicon Etcher, Veeco Savannah ALD, ReynoldsTech Cu ECD Hood, DC Probe Station, Microwave Small-Signal Probe Station

Abstract:

As the demand for heterogeneous-integrated RF chips increases, interposers for millimeter-wave circuits using through-silicon vias (TSVs) have become increasingly important due to their low loss and high-power capacity even at extremely high frequencies. For frequencies above 110 GHz, substrate-integrated waveguides (SIWs) are small enough to be integrated in Si interposers for high-power interconnects.

They can also be used to form high-quality passive devices such as filters and antennas, which have been difficult to integrate on-chip. This enables system-on-chip. In this study, we investigate the fabrication of SIWs and grounded coplanar waveguides (GCPWs) in Si interposers with a thickness of around 200 µm with resistivities ranging from 10-10000 Ω·cm. Thin Si wafers were patterned and etched using the Bosch deep reactive ion etching (DRIE) process to create TSVs. The TSVs were then metallized with platinum (Pt) using atomic layer deposition (ALD) and filled with copper (Cu) using electroplating deposition, before patterning the frontside.

DC measurements confirm a TSV series resistance of less than 1Ω. Small-signal millimeter-wave-on-wafer measurements show that the coplanar interconnects fabricated on high-resistivity (HR, ρ > 1000 Ω·cm) Si have an insertion loss of 0.7 dB/mm at 40 GHz, an order of magnitude better than the same coplanar interconnects fabricated on doped Si (ρ > 10 Ω·cm).

Summary of Research:

Si is the most extensively used material in semiconductor devices due to its exceptional electrical and mechanical properties, including a high dielectric constant, electrical resistivity, breakdown strength, and low loss tangent. These characteristics, and its cost effectiveness, make it an attractive candidate for SIWs. However, its relatively low mechanical toughness and high thermal conductivity compared to materials like silicon carbide (SiC) pose challenges during processing, particularly in etching processes. Our group has previously demonstrated SiC as a viable substrate material for SIW processing, and we adapted the same methodology as a proof of principle for Si SIW fabrication.

To develop a processing recipe for Si-based SIWs, we used a thinned HR Si wafer with a thickness of approximately 200 µm and resistivity greater than 1000 Ω·cm. Building on a similar methodology used for SiC SIWs while taking advantage of the more advanced etching processes available for Si, we began by depositing a 50 nm layer of aluminum oxide (Al2O3) on the wafer's backside using AJA Sputter deposition. Al2O3 was selected as the etch mask due to its excellent masking performance in the Bosch DRIE process for Si, providing a high selectivity greater than 1:1000.

The DRIE was performed using the UNAXIS 770 Deep Silicon Etcher. The etching chemistry employed C4F8 and SF6, which react with Si to anisotropically form vias. As shown in Figure 1, this process yielded 200 µm-deep TSVs with a diameter of 50 µm and sidewall angles ranging from 80 to 90 degrees.

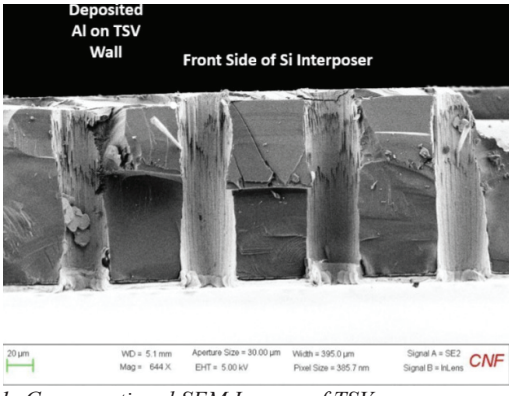

Figure 1: Cross-sectional SEM Images of TSVs.

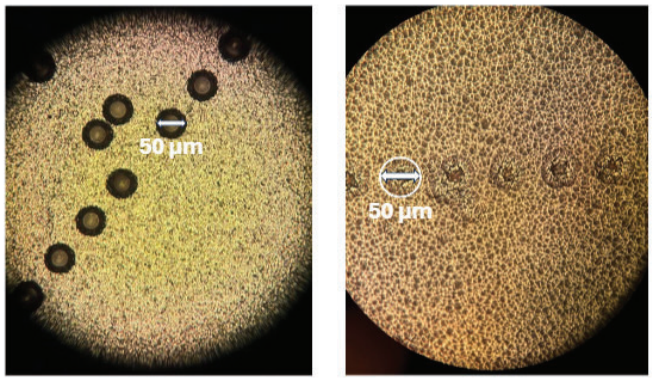

Figure 2: Top-View Optical Image of TSVs After 3 and 12 Hours of Cu Electroplating.

After the TSVs were fully etched through, ALD was used to coat the TSV sidewalls with a Pt seed layer, functioning also as an effective diffusion barrier and adhesion layer. Cu was then electroplated to fill the TSVs, initiating from the Pt seed layer, as illustrated in Figure 2.

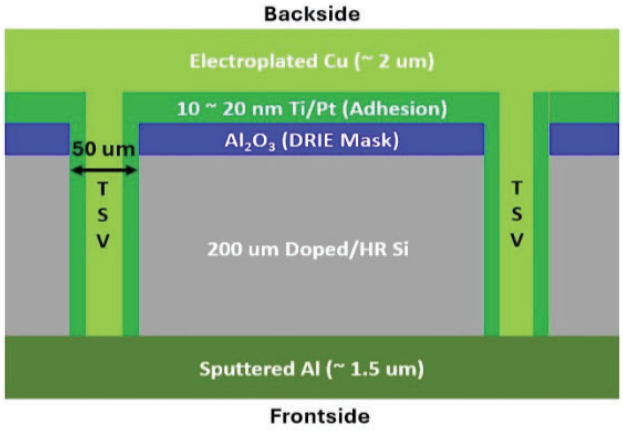

Figure 3: Schematic of Si Interposer Layout.

Once the backside processing was completed, the front side was patterned with SIW and GCPW lines. A platinum/aluminum (Pt/Al) layer was subsequently deposited using AJA Sputter deposition to complete the vertical interposer pathway. The structural details and final device configuration is depicted in Figure 3.

Both HR and doped Si devices were tested at the High Frequency Test Lab (HFTL) where TSV series resistance and GCPW line performance were evaluated. Using the DC probe station, I-V measurements showed that the TSV series resistance was typically below 1Ω for both HR and doped Si substrates. I-V curves also confirmed a resistivity ranging from 4.7 to 17.4 kΩ·cm, confirming that high resistivity of the HR Si substrate. RF measurements were then conducted over the 1-40 GHz range using the small-signal probe station, as shown in Figure 4.

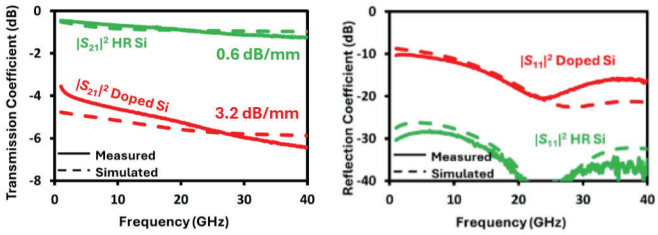

Figure 4: Measured Insertion Loss (S21) and Return Loss (S11) of Doped and HR Si Substrates Across 1-40 GHz.

For HR Si, the insertion loss (S21) value was approximately 0.7 dB/mm, with return loss (S11) exceeding 20 dB. In comparison, doped Si devices exhibited a much higher insertion loss of approximately 3.2 dB/mm and a return loss greater than 10 dB.

Conclusions and Future Steps:

The fabrication of Si interposers focused on optimizing Bosch DRIE of thinned Si wafers and refining metallization processes to achieve uniform anisotropic etching and consistent metal filling across the wafer. Measurements comparing HR and doped Si substrates revealed that HR Si shows insertion losses an order of magnitude lower than the doped Si, highlighting its potential as a promising substrate material for millimeter-wave applications. Looking ahead, with updated tools and improved techniques for etching and metallization, fully metal-filled TSVs are expected to achieve insertion losses below 0.5 dB/mm at frequencies up to 220 GHz, utilizing the 220 GHz single-sweep probe station at HFTL; once these targets are achieved, our group hopes to achieve heterogeneous integration in the cleanroom with flip chip bonding.

References:

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