Area-Selective Deposition to Enable Single-digit nm Fabrication

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Primary CNF Tools Used: Photolithography spinners and hotplates, GCA AS200 stepper, Oxford 81/82 (80+) RIE etchers, Anatech resist strip, CVC SC4500 e-beam evaporator (odd), Logitech Orbis CMP

Abstract:

As semiconductor manufacturing approaches single-digit nm feature sizes, there is an increasing difficulty in reliably patterning critical device features. A major obstacle is that conventional top-down techniques suffer from issues with alignment of device features during the manufacturing process. Area-selective deposition (ASD) seeks to remedy this by a bottom-up technique; selectively depositing films only on defined growth areas and not on non-growth regions, creating a "self-aligned" feature. We produce line and space patterned wafers of metal and dielectric, copper and silicon dioxide in this study, to serve as a substrate for ASD experiments. We use various characterization techniques, such as optical microscopy and scanning electron microscopy (SEM), to evaluate our wafers. We also discuss intended uses of these wafers in ASD experiments.

Introduction:

For decades, top-down manufacturing has been the method of choice for fabricating semiconductor devices. However, as we approach single-digit nm feature sizes, device patterning becomes problematic. At this scale, pattern misalignment can severely affect device functionality and operation. This misalignment is known as the "edge placement error" [1], which is defined as the distance between the actual and intended position of a patterned feature. ASD could achieve device patterning at the single-digit nm scale by utilizing a bottom-up approach, selectively depositing thin films using atomic layer deposition (ALD) or chemical vapor deposition (CVD) on defined deposition areas. By depositing thin films only on intended areas, any possibility of misalignment could be eliminated, because a "self-aligned" feature is created. In addition to resolving feature misalignment, ASD also introduces advantages such as uniform, conformal, and angstrom level thickness-controlled deposition of thin films.

In this study, 10, 5, 3, and 1 μm line and space patterns of copper (Cu) and silicon dioxide (SiO_2) were fabricated to study ASD of thin films. Alternating metal and dielectric patterns allow investigation of ASD of thin films on Cu and not on SiO_2, or vice versa. Variable widths of Cu and SiO_2 enable study of how film growth varies with different feature sizes. The pattern also has equal line and space widths of Cu and SiO_2, producing a 50/50 area coverage of metal and dielectric for *in situ* X-ray photoelectron spectroscopy (XPS) studies.

Experiment Details:

500 nm SiO_2 on 100 mm Si wafers were utilized. Wafers were cleaned in a Hamatech automated wafer processer with piranha solution before spin coating. Brewer Science WiDE-C 15C bottom anti-reflective coating (BARC) was spun at 3000 RPM for 60 seconds before a two-step bake on a 190°C proximity hotplate for 60 seconds, followed by a 160°C vacuum hotplate for 60 seconds. OiR 620-7i photoresist was spun at 5000 RPM for 60 seconds followed by a pre-exposure 90°C vacuum hotplate bake for 60 seconds. Exposure was performed on a GCA AS200 stepper, followed by a post-exposure bake on a 115°C vacuum hotplate. Etching was preformed using an Oxford 80+ reactive ion etcher. BARC was etched using an O_2 and Ar mixture for six minutes. SiO_2 was etched with a mixture of CHF_3 and Ar for 6:30 minutes to etch ~ 220 nm into the SiO_2.

Resist and BARC were stripped using an Anatech O_2 plasma dry strip, followed by a piranha clean. The CVC SC4500 e-beam evaporator was then used to deposit 25 nm of Ta as an adhesion layer, followed by 300 nm Cu. Logitech-Orbis CMP was finally used to planarize the surface and remove Cu overburden at 4 psi down and 30 psi back pressure for 1:50 minutes. The Hamatech was then used again to clean wafer of CMP debris.

Results and Discussion:

Optical microscope images showed a definite line and space pattern of Cu and SiO_2. Images confirm enough Cu overburden was polished away to reveal the desired pattern, as shown in Figure 1. Cross-sectional SEM images show the anisotropic etch profile, and the Cu and Ta layers deposited in Figure 2.

Ta was deposited as an adhesion layer between the Cu and the SiO_2. Without Ta, Cu would rip out of the trenches during the CMP step due to its poor adhesion to SiO_2.

No metal was seen on top of the SiO_2, and the Cu line was level with the SiO_2 space. Etch depth and anisotropic profile was consistent across varying feature sizes, as shown in Figure 3. The depth of Cu was kept greater than 70 nm, thick enough to serve as a substrate layer for surface-sensitive analysis techniques such as XPS. CHF_3 and Ar was chosen as the etch chemistry for its anisotropic etch profile. The gas mixture combined physical etching from Ar and chemical etching from CHF_3.

CHF_3 provides F radicals that etch SiO_2 [2,3]. Ar+ ions etch the SiO_2 by breaking its crystal bonds. Ar+ also desorbs the fluoropolymer film generated by the CHF_3 radicals, exposing horizontal surfaces to the etch gases [2]. The fluoropolymer keeps the etch directional, by passivating the sidewalls of the SiO_2 preventing lateral etching.

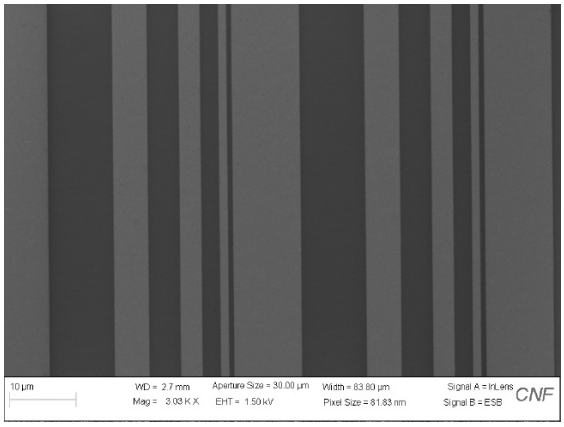

Figure 1: Top-down optical microscope image of 10, 5, 3, and 1 µm widths of Cu and SiO_2. Bright areas correspond to Cu and dark areas to SiO_2.

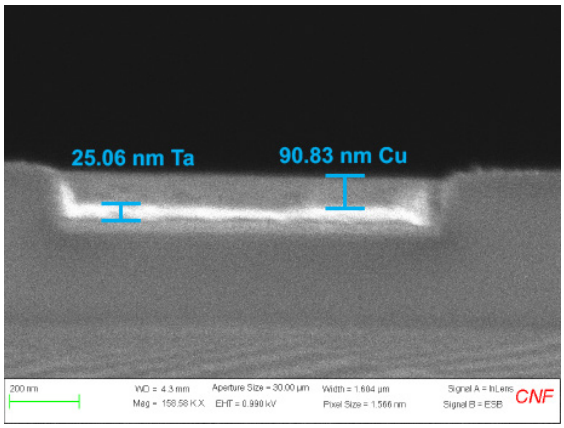

Figure 2: Cross-sectional SEM image of a 1 µm width trench filled with 90.83 nm Cu on top of 25.06 nm Ta.

Conclusions:

We successfully developed a robust and reproducible process to fabricate patterned line and space wafers. The ability to perform experiments on a patterned wafer will greatly enhance our understanding of area selective deposition.

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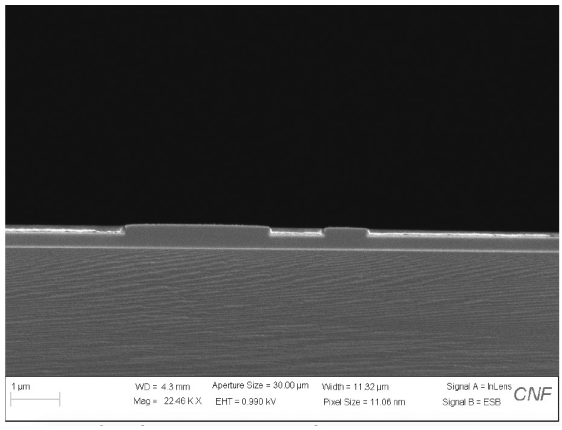

Figure 3: Etch uniformity across varying feature sizes.