Fabrication of Fluxonium-Like Qubits

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Primary CNF Tools Used: ASML DUV Stepper, JEOL 6300, PT770 Plasma Etcher, Heidelberg DWL2000 Mask Writer

Abstract:

In the drive for a scalable qubit-based processor, one of the most important resources is the ratio between qubit lifetime and gate operation time. Superconducting qubits provide a promising avenue for such a processor. Fluxonium qubits are exciting candidates in particular, having larger coherence times than the conventional transmons due to reduced sensitivity to several noise channels. Fluxonium qubits are intrinsically protected against charge noise due to the large inductive chain shunting the two capacitor pads, and protected against flux noise at the two flux sweet spots. Some of these qubits have lifetimes exceeding a millisecond, with gate times on the order of nanoseconds [1]. This project's fluxonium-like qubits are fabricated using an established recipe [2].

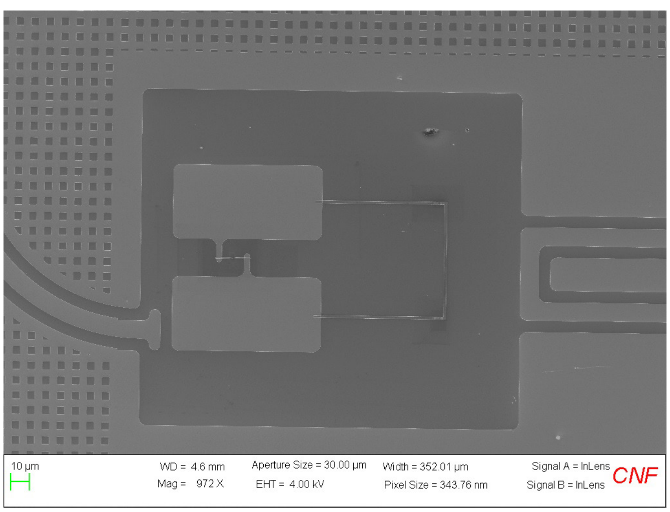

Figure 1: Scanning electron microscopy (SEM) image of one of the fluxonium qubits taken at CNF.

Summary of Research:

A fluxonium qubit is composed of a capacitive element, with a Josephson junction shorting the capacitive element. The key difference between a fluxonium and the more commonly studied transmon qubit is the inclusion of an inductor made of a chain of Josephson junctions, which shorts the two capacitor pads (Figure 1). This forms a closed loop for flux to thread through. This qubit is capacitively coupled to a resonator, whose frequency is shifted based on the state of the fluxonium qubit.

The devices are designed to facilitate direct control of each qubit on chip. For each device, there is one flux line per fluxonium and one charge bias line per transmon. These chips also utilize direct microwave drive lines to the individual qubits. Flux traps are etched across the entire ground plane of the chip, to limit the interaction of stray magnetic vortices with the fluxonium qubits. The resonant frequencies of the co-planar waveguide resonators on the chip are carefully chosen to ensure effective coupling with the qubits and easy measurement with the lab electronics. Test structures are distributed along the chip's edges, allowing for post-fabrication checks on the quality of electron-beam lithography and evaporation.

The fluxonium qubits are fabricated first by depositing a layer of niobium on a silicon wafer at Syracuse University using sputtering. The Heidelberg DWL2000 is used to construct a photomask equipped with various modular components to allow for tuning of circuit parameters after the design is finalized. Each of the chips is fabricated with two fluxonium and two transmon qubits. Frequencies for both of the qubits are targeted to be the same so that the properties of the two different qubit architectures can be compared. They are fabricated simultaneously on the same chip to reduce the factors related to fabrication variability.

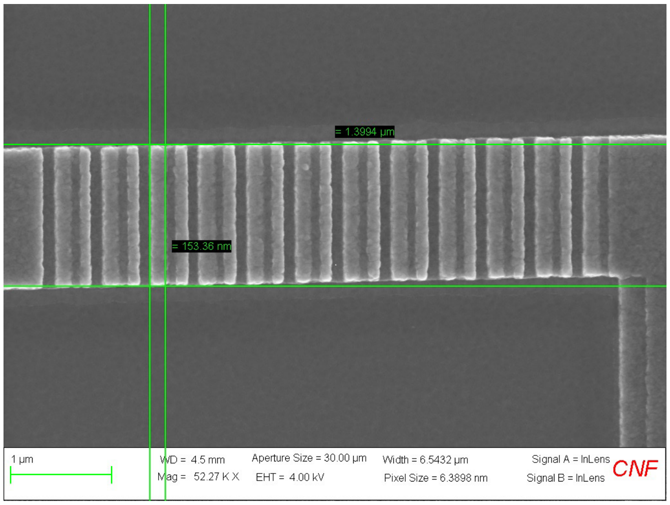

Figure 2: SEM image of a Josephson junction chain, taken at CNF.

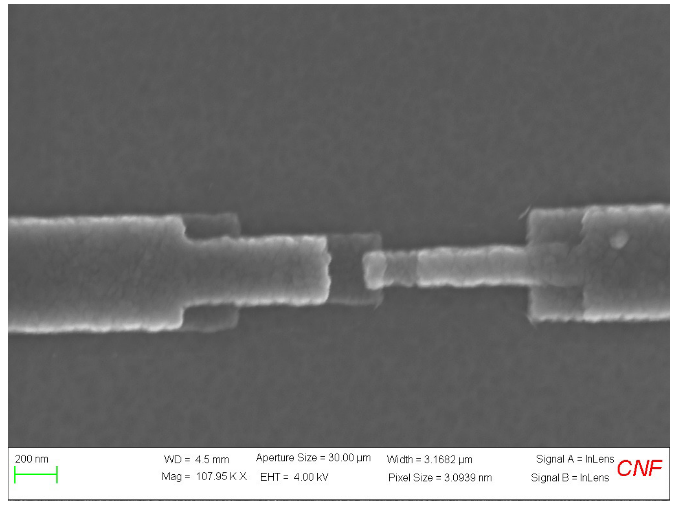

Figure 3: SEM of a single small Josephson junction, taken at CNF.

The base layer pattern (including the readout resonators, capacitor pads for the fluxonium and the transmon qubits, as well as the readout coplanar waveguide) is patterned into this niobium layer with the ASML DUV stepper. The wafer is then developed and cleaned before having the pattern etched into the superconducting niobium with the PT770. To remove oxides that may degrade the qubit performance, an additional HF cleaning step is done, after which the wafer is prepared for electron-beam lithography. After the electron-beam lithography pattern is developed, the device will have bridges formed of the remaining resist, which enables double-angle shadow evaporation for making the Josephson junctions. The lower pads for the Josephson junctions are deposited first, then the junctions are oxidized, and finally, the upper pads are deposited (Figure 2). This is all done with only a single electron-beam lithography.

The technique can be used to form the chain of Josephson junctions that serve a role of an inductor and the singular small junction (Figure 3). This evaporation and the intermediate oxidation are done at Syracuse University.

After the small junctions and the junction chain have been formed, the devices are returned to CNF to be diced. These devices are measured at Syracuse University in a Bluefors dilution refrigerator at temperatures below 10 mK.

The goal is to develop the capability to target specific qubit parameters and to optimize said parameters for a higher energy relaxation T1 and phase coherence T2 times. These devices also will benefit from expanding the range of fabrication techniques used in the fabrication process, potentially further limiting loss and increasing qubit lifetimes.

References:

[1] A. Somoroff, et al. Millisecond Coherence in a Superconducting Qubit. Phys. Rev. Lett., 130, 267001 (2023). https://doi.org/10.1103/PhysRevLett.130.267001.

[2] V. Iaia, et al. Phonon downconversion to suppress correlated errors in superconducting qubits. Nature Communications, 13, 6425 (2022). https://doi.org10.1038/s41467-022-33997-0.