InAlN/GaN HEMTs on Si with Regrown Contacts and f_T/f_{MAX} of 250/204 GHz

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Primary CNF Tools Used: Autostep i-line stepper, Heidelberg mask writer DWL2000, P7 profilometer, FilMetrics, AFM Veeco Icon, Zeiss SEM, PT770, Oxford 81, Oxford PECVD, Oxford ALD, SC4500 evaporators, AJA sputter deposition tools, RTA AG610, JEOL 9500

Abstract:

Depletion-mode high-electron mobility transistors (HEMTs) based on a quaternary barrier $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructure on Si substrate were fabricated. The 55 nm long gate device shows a DC drain current density of 2.8 A/mm, a peak extrinsic transconductance of 660 mS/mm, and balanced current gain cutoff frequency f_T and maximum oscillation frequency f_{MAX} are 250 and 205 GHz, respectively.

Summary of Research:

Gallium nitride high electron mobility transistors (GaN HEMTs) have high breakdown voltages, high two-dimensional electron gas (2DEG) densities, and a high electron saturation velocity. These properties make them ideal for high-power and high-frequency applications, such as switches in power systems and amplifiers in wireless communication systems.

To date, the highest speed GaN HEMTs are demonstrated on SiC substrates, all of which employ regrown ohmic contacts to minimize source/drain resistances. In this report, we have demonstrated the high-frequency and high-power performance capacity of GaN HEMTs on Si substrates. The $I_{D,MAX}$, peak g_m and f_T-f_{MAX} product are among the best reported for GaN HEMTs on Si, which are very close to the state-of-the-art depletion-mode GaN HEMTs on SiC without a back barrier. This highlight celebrates advances on this front achieved in the CNF and published at IEEE Electron Devices Letters [1].

The InAlN/AlN/GaN HEMT structure consists of a 10 nm $In_{0.17}Al_{0.83}N$ barrier, a 1 nm AlN spacer (total barrier thickness: 11 nm), an 800 nm unintentionally doped GaN channel, and AlGaN/AlN buffer and nucleation layers on 200-mm-diameter Si substrate, grown by a Propel® HVM MOCVD system at Veeco Instruments. Room temperature Hall-effect measurements prior to device fabrication showed a 2DEG sheet concentration of $2.27 \times 10^{13}/cm^2$ and electron mobility of 1430 $cm^2/V{\cdot}s$, corresponding to a sheet resistance of 206 Ω/sq.

A schematic cross-section of the InAlN/AlN/GaN HEMT device with regrown n^+ GaN contacts is shown in Figure 1(a). The device fabrication process started with patterning of a SiO_2 mask for n^+GaN ohmic regrowth by PA-MBE. The preregrowth etch depth into the HEMT structure was 40 nm, and regrown n^+GaN was 100 nm with a Si doping level of 7×10^{19} /cm^3. Non-alloyed ohmic contact of Ti/Au/Ni was deposited by e-beam evaporation. T-shaped Ni/Au (40/200 nm) gates were formed by electron-beam lithography by JEOL 9500, followed by liftoff. TLM measurements yielded a contact resistance of 0.07 Ω·mm. The device presented here has a regrown n^+GaN source-drain distance L_{sd} of 175 nm, a gate width of 2 × 25 µm, and a gate length L_g of 55 nm. Figure 1(b) shows an angled-SEM image of the fabricated InAlN/AlN/GaN HEMT.

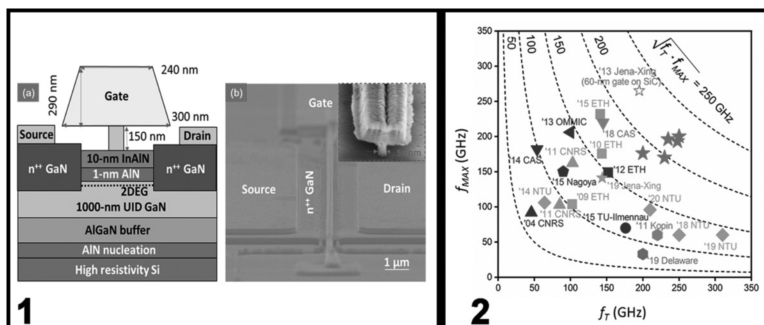

Figure 1, left; (a) Schematic cross-section of InAlN/AlN/GaN HEMTs on Si with regrown n^+GaN contacts. (b) An angled SEM image of a fabricated InAlN/AlN/GaN HEMT with an EBL T-gate. ***Figure 2, right:*** *Comparison of the measured f_T and f_{MAX} of GaN HEMTs on Si substrates. (See pages vi-vii for full color versions.)*

The observed maximum drain current $I_{D,MAX}$ of 2.8 A/mm and the on resistance R_{ON} of 0.6 Ω·mm, along with the peak transconductance g_m of 0.66 S/mm, are among the best in GaN HEMTs on Si, comparable to GaN HEMTs on SiC without a back barrier. At low V_{DS}, these HEMTs typically exhibit a decent I_{ON}/I_{OFF} ratio ~ 10^5; HEMT A has the highest gate leakage among all the tested devices, most likely due to processing non-uniformity. The f_T/f_{MAX} of 250/204 GHz are obtained after de-embedding in HEMT A; in comparison, neglecting the short de-embedding test structure renders similar f_T/f_{MAX} values of 245/187 GHz. In Figure 2, the f_T and f_{MAX} values achieved in this work are compared to other reported GaN HEMTs on Si, as well as the state-of-the-art GaN HEMTs on SiC with similar epi-structures and device dimensions (gate length, barrier materials, and its thickness, no back barrier). It can be seen the present HEMTs are clustered near the upper right corner as desired, with $(f_T \cdot f_{MAX})^{1/2}$ very close to that of the GaN HEMTs on SiC with a comparable gate length.

GaN HEMTs on Si with different geometries were fabricated, measured, and analyzed. The analysis confirms the benefits of n^{++}-GaN source/drain contacts and T-shaped gates, especially in achieving both high f_{MAX} and f_T. With the state-of-the-art regrown ohmics, scaled source-drain separation and T-gates, GaN HEMTs on Si achieve comparable metrics with that on SiC in terms of DC and small-signal performance.

References:

[1] L. Li, K. Nomoto, D. Jena, H. G. Xing, et al., “GaN HEMTs on Si with Regrown Contacts and Cutoff/Maximum Oscillation Frequencies of 250/204 GHz”; IEEE Electron Device Lett., 10.1109/LED.2020.2984727, March. 2020.

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