Ultra-Wide Bandgap Power Electronic Devices

CNF Project Number: 2800-19

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Primary Source(s) of Research Funding: NSF DMREF Program under Grant 1534303, AFOSR under Grants FA9550-17-1-0048, FA9550-18-1-0529 and FA9550-18-1-0479

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Primary CNF Tools Used: Oxford PECVD, Oxford ALD, odd-hour and even-hour evaporator, AJA sputtering tool, PT-770 etcher, Oxford 81 etcher, Gen-1000 etcher, UV-Ozone, Autostep i-line stepper, ABM contact aligner, Heidelberg mask writer-DWL2000, AFM-Veeco Icon, Oxford ALD FlexAL

ELECTRONICS

Abstract:

Ultra-wide bandgap semiconductor materials, such as beta-phase gallium(III) trioxide (Ga_2O_3), have unprecedentedly high breakdown electric field, thus are considered very promising for use in power electronic devices. Through ingenuous design of the device structure and material interface, we successfully demonstrated high-voltage, low-loss vertical Ga_2O_3 Schottky barrier diodes and fin transistors with record-high performance. The device breakdown voltage shows a significant improvement with the employment of the field-plate technique as edge termination.

Summary of Research:

Beta-phase Ga_2O_3 has been under intensive research as a promising ultrawide-bandgap semiconductor material. It is expected to have a high breakdown electric field of up to 8 MV/cm due to the sizable bandgap of 4.5-4.7 eV, as well as a decent electron mobility of up to ~ 200 $cm^2/V \cdot s$. These properties yield a Baliga's power figure-of-merit higher than GaN and 4H-SiC, thus making Ga_2O_3 a strong material candidate for high power devices. In addition, melt-growth techniques for Ga_2O_3 substrates are available, which promises a cost-effective device platform.

Previously, we have successfully demonstrated Ga_2O_3 trench Schottky barrier diodes with a breakdown voltage (BV) of 2.44 kV [1]. In addition, we realized enhancement-mode vertical fin transistors with a breakdown voltage over 1 kV [2]. Despite the promising performance, the figure-of-merit of the previous devices are still far from the material limit of Ga_2O_3. One of the major reasons is the electric field crowding at the edge of the devices, which leads to premature breakdown. In this work, we improved upon the previous devices by adopting the field plate technique for more effective edge termination.

The fabrication process flow of the field-plated trench Schottky barrier diode prior to the addition of the field plate is largely the same as reported previously. The vertical fin channels were first formed by dry etching using PT-770 etcher. Then, Ti/Au (75/150 nm) cathode ohmic contact was deposited by e-beam evaporation, followed by the deposition of the first Al_2O_3 dielectric of 105 nm by atomic layer deposition using the Oxford ALD tool. After opening of the Al_2O_3 on top of the fin channel by dry etching, Ni (30 nm) Schottky contact and then Ti/Pt (40/40 nm) sidewall coverage were deposited by electron-beam evaporation and sputtering, respectively. To form the field plate, a second ALD Al_2O_3 dielectric layer of 125 nm was deposited. Then, contact holes were formed by dry etching to expose the anode metal. Lastly, the Ti/Al/Cu/Au (10/70/10/60 nm) field-plate metal stack was deposited.

The fabrication process for the field-plated Ga_2O_3 vertical fin transistors is as follows: An n^+ layer was formed on the top surface by Si-implantation and activated at 1000°C to facilitate the source ohmic contact. Submicron fin channels were defined by electron beam lithography and formed by dry etching using a BCl_3/Ar mixture. The resultant fin channels have a near vertical sidewall profile. After dry etching, the Cr/Pt etch mask was removed by Cr etchant and the wafer was treated with HF for 23 min to remove plasma damage. Next, the drain contact (Ti/Au) was deposited before the deposition of the gate stack, consisting of a 35 nm Al_2O_3 gate dielectric by atomic layer deposition (ALD) and a 50-nm Cr gate by sputtering. The gate stack and thick ALD Al_2O_3 spacer was patterned by photoresist planarization and

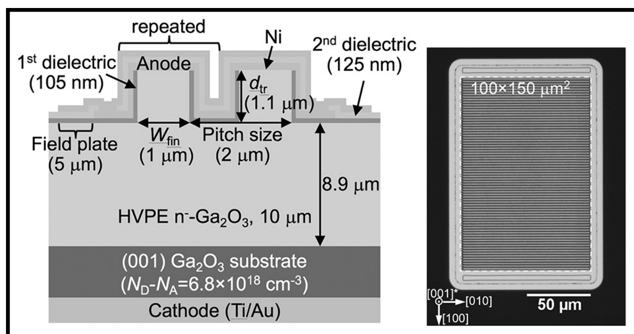

Figure 1: Schematic cross-section and optical top view of the field-plated Ga_2O_3 trench Schottky barrier diodes.

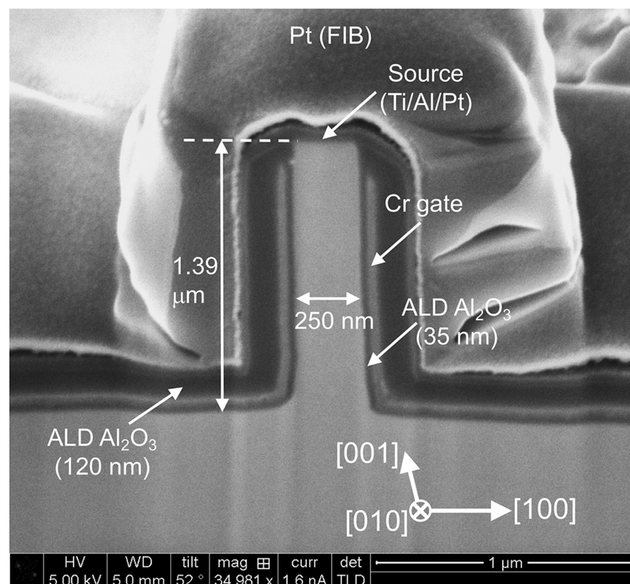

Figure 2: SEM cross-section of the field-plated Ga_2O_3 vertical fin transistors.

self-aligned etching processes detailed in our previous reports. The source electrode (Ti/Al/Pt) was deposited by sputtering after the spacer formation, simultaneously forming the source-connected field-plate.

The field-plated trench Schottky barrier diodes have a specific on-resistance of 10.5 mΩ·cm^2. In comparison with the regular SBDs, the field-plated trench SBDs have much lower leakage current as well as a much higher breakdown voltage of 2.89 kV. With addition of the field plate, the destructive breakdown voltage increases by ~ 500 V.

The field-plated trench SBD in this work achieves a power figure-of-merit (BV^2/R_{on}) of 0.80 GW/cm^2 from DC measurements, which is the highest among all Ga_2O_3 power devices to date [3].

The vertical Ga_2O_3 fin transistors exhibit normally-off operation and a threshold voltage of 1.8 V with a fin channel width of 0.15 µm. The device has an on-off ratio of > 10^8 and a V_{th} of ~ 1.8 V at 0.1 A/cm^2. The R_{on} is determined to be 25.2 mΩ·cm^2 from DC measurements. The field-plate helps boost the 3-terminal breakdown voltage from 1 kV to over 2.6 kV, a record high among all Ga_2O_3 transistors [4].

In summary, we have demonstrated improved performance in Ga_2O_3 power diodes and transistors, by using a field-plate technique, marking a significant step forward in the development of high performance Ga_2O_3 power transistors.

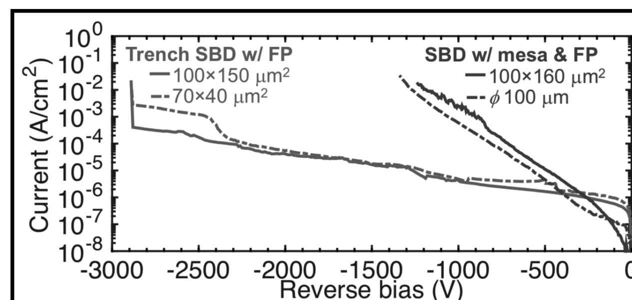

Figure 3: Reverse I-V characteristics of the field-plated Ga_2O_3 trench Schottky barrier diodes.

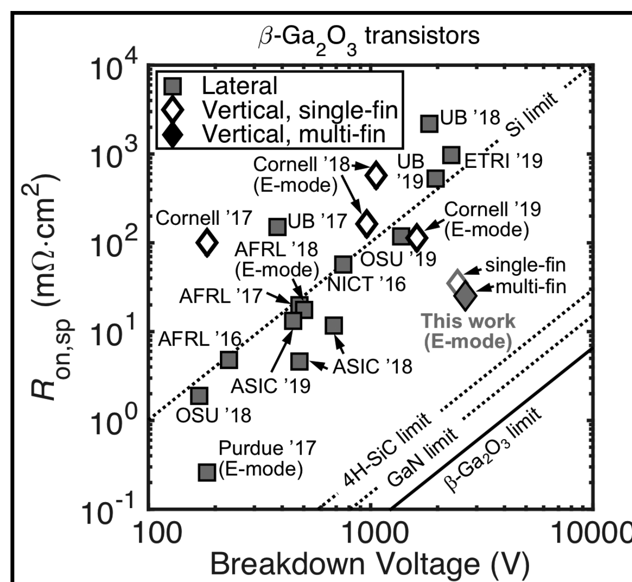

Figure 4: Performance of the field-plated vertical fin transistors in comparison with literature reports.

References:

[1] W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, 2018 IEEE International Electron Devices Meeting (IEDM), pp. 8.5.1, 2018.

[2] Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, IEEE Electron Device Lett. 39, 869 (2018).

[3] W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, IEEE Electron Device Lett. 41, 107 (2020).

[4] W. Li, K. Nomoto, Z. Hu, T. Nakamura, D. Jena, and H. G. Xing, 2019 IEEE International Electron Devices Meeting (IEDM), pp. 12.4.1, 2019.