$PtSe_2$ RF MOSFETs and CMOS Integration

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Primary CNF Tools Used: ABM contact aligner, Autostep i-line stepper, Oxford PlasmaLab 80+ plasma reactor, SC4500 odd-hour evaporator, Oxford atomic layer deposition (ALD)

Abstract:

Few-layer platinum diselenide ($PtSe_2$) is attractive because it has a sizable bandgap, high carrier mobility, air stability, and can be synthesized below 450°C by thermal conversion or molecular beam epitaxy (MBE). In addition, bulk $PtSe_2$ is a semimetal, which can facilitate low-resistance contacts—a challenge for all 2-D devices to date. Taking advantage of these unique properties, we reported CMOS-compatible ultralow-contact-resistance $PtSe_2$ MOSFETs [2]. However, these devices suffer from poor gate modulation due to the relatively thick $PtSe_2$.

To improve gate modulation, we fabricated MOSFETs on trilayer $PtSe_2$ grown by MBE. The MOSFETs are *n*-type with a current on/off ratio of 43 and 1600 at 290 and 80 K, respectively. These results are among the best of transistors based on synthesized $PtSe_2$. Despite the thin $PtSe_2$ layer, doping by contact bias lowers the contact resistance significantly and boosts the current capacity and the on/off current ratio. Temperature-dependent current-voltage characteristics imply a bandgap of approximately 0.2 eV for trilayer $PtSe_2$, which confirms that the semiconductor-semimetal transition of $PtSe_2$ is not as abrupt as originally predicted.

Summary of Research:

Fabrication. The fabrication process is similar to [2] except for the $PtSe_2$ synthesis methods. The detailed structure of a single device is shown in Figure 1(a). After the deposition of Al_2O_3 as the gate dielectric, the chip was cleaned by acetone, isopropyl alcohol, and deionized water, before drying with N_2.

After it was loaded into a DCA Instruments R450 MBE reactor, it was outgassed for 30 min at 130°C, Growth commenced at 200°C under a Pt flux of $9.2 \times 10^{12}/cm^2 \cdot s$ and an Se flux of $1.6 \times 10^{14}/cm^2 \cdot s$. The Pt and Se fluxes are generated by an electron gun and a Knudsen cell, respectively. After growing for 339 s under both Pt and Se fluxes, the $PtSe_2$ was annealed at 400°C for 30 min under the Se flux alone to enhance its crystal quality.

The resulting $PtSe_2$ is approximately three monolayers (2-nm thick) and (001)-oriented with a high degree of in-plane rotational twin formation.

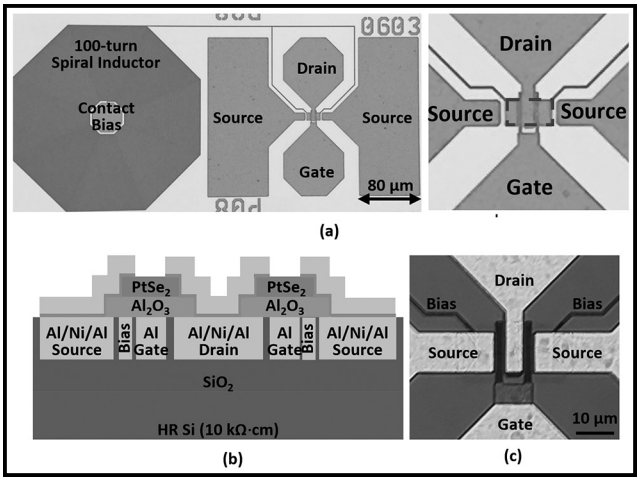

Figure 1: (a) Optical micrograph of individually probable RF MOSFET with source contact biased through a spiral inductor. (b) Cross section schematic. (c) Top-view micrograph of a finished $PtSe_2$ MOSFET.

The trilayer $PtSe_2$ was patterned by photolithography and etched outside the active region by an Oxford PlasmaLab 80+ plasma reactor for 5 s. The flow rates of CF_4 and O_2 were 100 and 20 sccm, respectively. The RF power was 200 W. After $PtSe_2$ etch, the photoresist was stripped by acetone for 30 min. Ni and Al contact layers 50- and 150-nm-thick, respectively, were evaporated by an electron gun.

Figures 1(b) and 1(c) show the cross-section schematic and the top-view micrograph, respectively, of a finished $PtSe_2$ MOSFET.

DC Performance. Figure 2(a) shows the total resistance R_T measured on transfer-length-method (TLM) test structures of different channel lengths. The extraction yields a sheet resistance R_{SH} = 1 × 10^8 Ω/5g and a contact resistance R_C = 2 × 10^8 Ω·μm. Figure 2(b) shows the transfer characteristics of a $PtSe_2$ MOSFET with the drain-source voltage V_{DS} = 3 V and different source contact biases V_{BS}, which helps further reduce the contact resistance as has been demonstrated in [3]. It shows the MOSFET exhibits *n*-type conduction with an on/off ratio of 22. With V_{BS} increasing from 0 to 7.5 V, the on current of the drain I_D^{ON} increases from 60 to 130 nA, while its off current I_D^{OFF} remains the same at 3 nA. Thus, the on/off ratio increases from 22 to 43 mainly due to an increased I_D^{ON}. The results are comparable to $PtSe_2$ grown by chemical vapor deposition.

Thermal Dependence and Bandgap. Figure 3(a) shows the temperature-dependent transfer characteristics of a $PtSe_2$ MOSFET with V_{DS} = 3 V and V_{BS} = 7.5 V. With the ambient temperature decreasing from 290 K to 80 K, the on/off ratio increases from 43 to 1600. This is because I_D^{OFF} decreases much faster than I_D^{ON}, suggesting that they are governed by different activation energies. This difference is confirmed by the Arrhenius plots Figure 3 (b) of the total channel conductance between 80 K and 290 K with V_{DS} = 3 V, V_{BS} = 7.5, and V_{GS} = -5, 0, or 7 V.

The activation energy E_A decreases from 0.18 eV at V_{GS} = -5 V to 0.11 eV at V_{GS} = 7 V. Therefore, the off-state E_A of 0.18 eV should be more indicative of the bandgap of trilayer $PtSe_2$ instead of the on-state E_A.

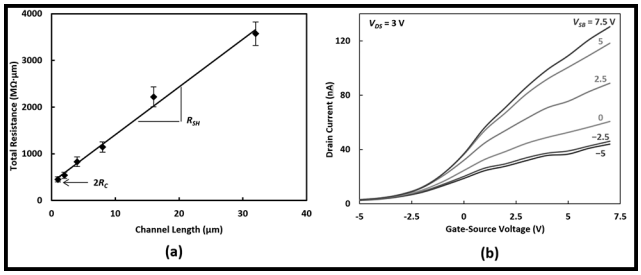

Figure 2: (a) TLM results. (b) Transfer characteristics of a $PtSe_2$ MOSFET under different source contact biases.

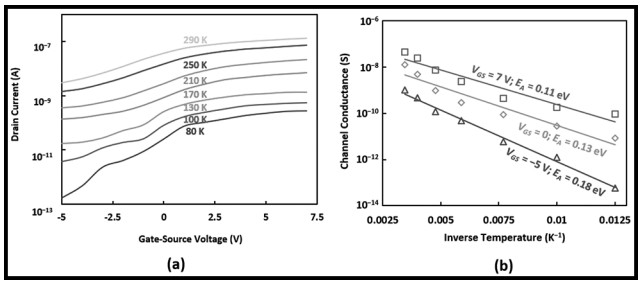

Figure 3: (a) Transfer characteristics of a $PtSe_2$ MOSFET at different temperatures. (b) Channel conductance of a $PtSe_2$ MOSFET between 80 and 290 K.

Future Directions:

First, better MOSFET performance can be expected by growing even thinner $PtSe_2$ uniformly and by thickening the $PtSe_2$ in the contact regions. Second, it is challenging to grow monolayer or bilayer $PtSe_2$ using either MBE or CVD methods. An alternative approach is to use a shadow mask to create the recessed $PtSe_2$ profile.

References:

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[2] L. Li, et al., "Wafer-scale fabrication of recessed-channel $PtSe_2$ MOSFETs with low contact resistance and improve gate control," IEEE Trans. Electron Devices, V65, #10, pp. 4102-08, Oct. 2018.

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