Nanoscale Periodic Pillar Feature Process Survival

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Primary CNF Tools Used: ASML 300C DUV, GCA 5x Autostep i-line stepper

Abstract:

The ASML 300C DUV and GCA 5x Autostep i-line stepper have been used in previous years to produce pillar and hole features with diameters ranging from 232 nm to 816 nm on fused silica and silicon wafers. Hole features are favored over pillar features because pillars are more susceptible to destruction during further wafer processing. It has been found that pillar features give optical performance up to 3.5 times higher than the hole features in spectral applications. For this reason, pillar feature fabrication with further front and backside wafer processing as well as diced die polishing was explored. For wafers that had additional metal layers patterned on the front and back side of the wafer yields of 71-79% was found with hole features and a wafer yield of 50% was found for pillar features. For wafers that had additional metal layers patterned on the front and back side of the wafer that also had an edge polished on each die after singulation had yields of 53-89% for hole features and 8% for pillar features. This reduction in wafer yield for wafers with pillars versus holes was consistent with the initial results reported last year.

Summary of Research:

In previous years a process for patterning nanophotonic pillar and hole structures was developed at CNF that used the ASML 300C DUV stepper as well as the GCA 5x Autostep i-line stepper. These features were etched into the substrate material using the patterned resist as an etch mask. The ASML 300C DUV stepper process has been used to pattern 4-inch borosilicate float glass wafers ("borofloat"), 4-inch fused silica wafers, and 4-inch silicon wafers. Pillar features like those shown in Figure 1 were fabricated with diameters ranging from 232 nm to 816 nm. Hole features were fabricated with design diameters ranging from 306 nm to 446 nm. Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. Photonic crystal geometry was examined in the SEM and photonic crystal performance was assessed optically via extraction of waveguided light.

For recent applications, nanophotonic patterning was mainly focused on holes versus pillars because pillars are more likely to become damaged in a way which renders them useless for our spectral application during further processing and wafer handling. In recent years, processing steps have been added to the wafer after nanophotonic crystal pattering to include both front and back side aluminum reflector layers. These added layers can be combined with single edge polishing after die singulation as shown in Figure 2. These added steps make the pillars more exposed to handing that could damage them. It has been found that pillars designed to the same diameter of corresponding holes give spectral responsively between 50% -350% higher over a range of inputs between 400-1000 nm for designs with a diameter of 446 nm. It is because pillars give such a greater spectral responsively, that they have again been investigated for the fabrication of monolithic optical bench die design which include the light-scattering nanophotonic pattern, reflectors, and polished angular light input.

In the previous reporting period, nanophotonic pillar structures with diameters of 612 nm and 816 nm were made in fused silica wafers with the intent of seeing how they would survive further processing to produce the monolithic optical bench die design. These pillars were patterned on fused silica wafers with the ASML 300C DUV and etched into the substrate using the resist as an etch mask. The 612 nm diameter pillar wafers then had aluminum sputtered onto the front and backside which was patterned via contact lithography plus liftoff. The wafer was then coated with a protective ion beam assisted physical vapor deposited SiO_2 coating layer,

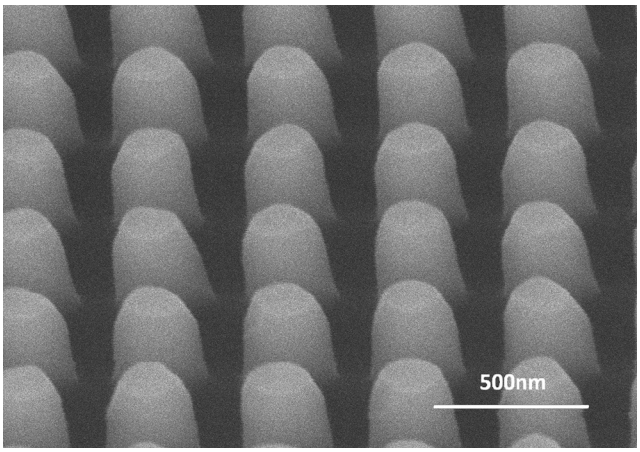

Figure 1: SEM image of photonic crystal pattern, nominally with 270 nm pillar features, fabricated fused silica with process developed with ASML 300C DUV stepper.

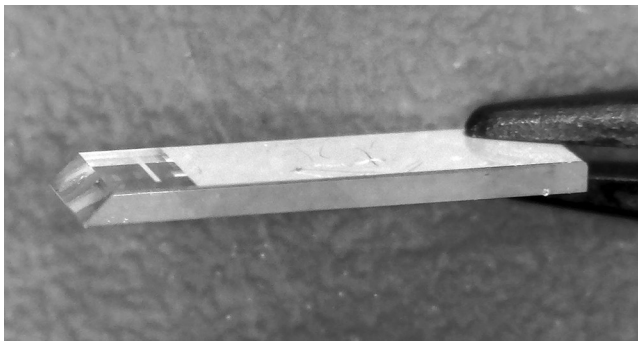

Figure 2: Diced and polished fused silica die with pattered Al reflectors on both sides in addition to the nanophotonic pattern and 45° edge polish.

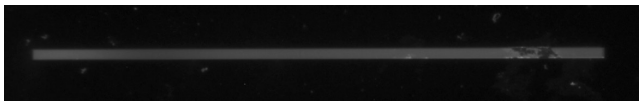

Figure 3: Green light (gray) being scattered through a 306 nm diameter nanophotonic pattern illuminating pillar damage.

Wafer Percent Yield with Additional Process Steps				
Wafer #	Nanostructure Type	Hole/Pillar Diameter	Metal Lift-Off on Both Sides	Metal + Polish
1	Hole	446nm	71%	
2	Hole	408nm	79%	
3	Pillar	612nm	50%	
4	Hole	498nm		89%
5	Hole	408nm		68%
6	Hole	408nm		82%
7	Hole	408nm		53%
8	Pillar	612nm		8%

Figure 4: Wafer percent yield with additional process steps and a variety of nanophotonic pattern diameters.

diced, optionally polished and cleaned. The resulting dies were inspected by waveguiding green light into the edge of the die and inspecting the nanophotonic crystal pattern in a microscope to check for defects. Pillar damage seen in this kind of inspection is apparent in the example given in Figure 3. Nanophotonic patterns may also be rejected for other kinds of defects.

A significant drop in photonic crystal yield was found for wafers with pillar nanophotonic patterns versus holes. Yield results are listed in the Figure 4 table. Wafers that only had metal patterning on the front and back had about 25% higher yield with holes versus pillar. Wafers that had edge polishing in addition to the front and back side metal patterning had an order of magnitude higher yield for wafers with holes versus pillars.

In summary, a process to fabricate nanophotonic pillar structures with a diameter of 612 nm has been used to make dies to with further processing including front and backside aluminum patterns and singulated die polishing. Although pillar features tend to be more fragile when it comes to further wafer processing, these features tend to give higher optical throughput in spectral scattering applications in spectrometer systems.

For wafers that had additional metal layers patterned on the front and backside of the wafer yields of 71-79% was found with hole features and 50% for pillar features. For wafers that had additional metal layers patterned on the front and backside of the wafer and also had an edge polished on each die after singulation yields of 53-89% was found with hole features and 8% for pillar features.