III-N Photonic Devices

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Principal Investigator(s): Debdeep Jena

User(s): Kevin Lee, Shyam Bharadwaj, Ryan Page, Jimy Encomendero

Affiliation(s): Electrical and Computer Engineering, Materials Science Engineering; Cornell University

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Contact: djena@cornell.edu, sb2347@cornell.edu, kl833@cornell.edu, rlp238@cornell.edu, jje64@cornell.edu

Primary CNF Tools Used: ABM contact aligner, electron-beam evaporators, Plasma-Therm inductively coupled plasma reactive ion etcher (PT 770), electron-beam lithography, atomic layer deposition, plasma-enhanced chemical vapor deposition

Abstract:

Lifi communication using III-Nitrides visible light sources has drawn huge attention recently. Our goal is to build monolithic integration of field effect transistor (FET) with blue light emitting diodes (LEDs). We use plasma-assisted molecular beam epitaxy (PA-MBE) to grow a buried tunnel junction blue LED with a n-i-n channel sitting on top. The resulting device we called "light emitting FET (LEFET)" shows successful gate modulation and on/off ratio of five orders. Light output signal can be switched up to 30 kHz.

Summary of Research:

The LEFET structure is grown on a n-type metal polar free-standing GaN substrate with dislocation density ~ 10^6 cm^{-2} by PA-MBE. The detailed structure is presented in Figure 1(a). First, a 125 nm Si-doped GaN layer is grown with [Si] = 10^{19} cm^{-3}. After initial n-GaN layer, p-GaN with Mg doping of 3 × 10^{19} cm^{-3}. This completes the buried tunnel junction for hole injection. The active region contains three periods of InGaN multiple quantum wells (MQWs) with blue emission at 467 nm. Later, the n-i-n FET region is grown using unintentional doped GaN (uid-GaN) sandwiched between two n-GaN layers.

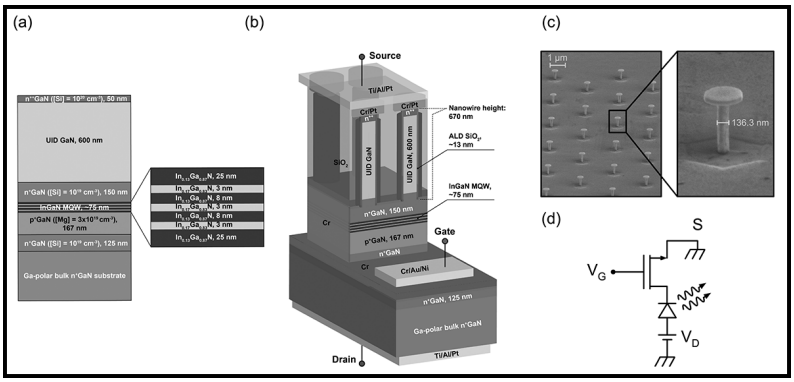

Figure 1: (a) Schematic epitaxial layer structure for the device discussed in this study. The structure consists of a vertical n-i-n GaN FET sitting above a bottom-TJ homojunction InGaN LED. (b) Schematic of a fabricated nanowire LEFET structure, showing source, gate, and drain contacts for biasing the device, and dielectrics for isolation. (c) SEM image of the nanowire LEFET structure. (d) Circuit diagram of the LEFET.

The sample was processed into devices consisting of various numbers of vertical n-FET nanowires or fins of varying dimensions on top of 55 × 55 μm^2 LED mesas.

A schematic of a processed nanowire LEFET is shown in Figure 1(b). First, 55 × 55 μm^2 LED areas were isolated through inductively-coupled plasma reactive ion etching (ICP-RIE) down to the n^+GaN nucleation layer. Next, nanowires and fins were defined on the mesa surface through electron beam lithography (EBL).

The etch process for nanowire/fin definition consisted of first an ICP etch (using Cr/Pt as an etch mask as well as top source contact) followed by a wet etch in AZ400K to make the sidewalls vertical for efficient lateral gating (see Figure 1(c)). The fins were defined with long edge along the m-plane direction in order to allow for adequate wet etching. Then, SiO_2 was deposited by atomic layer deposition (ALD) as a gate dielectric for the nanowire/fin FETs.

Next, Cr was sputtered as the sidewall gate metal, followed by e-beam evaporation of large Cr/Au/Ni pads for electrically contacting the gate. The undesired sputtered Cr above the source contact of the fins and wires was etched away after a planarization process, after which SiO_2 was blanket deposited by plasma-enhanced chemical vapor deposition (PECVD) to isolate

the rest of the sidewall gate metal. This SiO_2 was then planarized to again expose the Cr/Pt wire/fin source contact, after which thick source pads (Ti/Al/Pt) for probing were deposited. Gate isolation for the FET wires/fins between different devices (which still had their gates shorted together by the sputtered Cr at this point) and contact holes for the thick gate pads were realized together with an SiO_2 etch followed by a Cr etch.

Finally, a Ti/Al/Pt back contact was deposited with a window left free of metal for collecting light from the back side.

After device processing, electrical and optical measurements were performed, with results for a 500 nm × 50 µm single-fin device shown in Figures 2 and 3, respectively. Circular transfer length method (cTLM) measurements shown in Figure 2(a) reveal low contact and sheet resistances: 9.34×10^{-6} Wcm^2 for the top source contact, and 185 Ω/sq for the $n^{++}GaN$ contact layer underneath, resulting in negligible voltage drops across these regions. I_D-V_G and I_D-V_D measurements on the 500 nm × 50 µm single-fin device are shown in Figures 2(b) and (c), respectively, with current density values shown on the plots normalized to the area of the finFET.

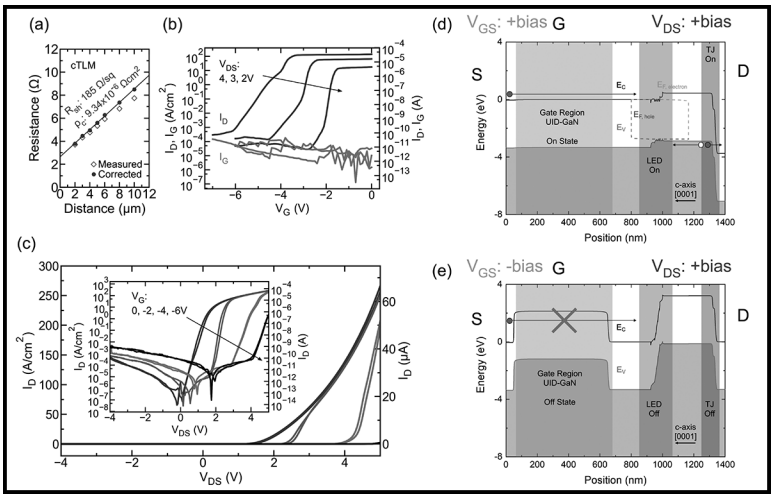

Figure 2: (a) Circular TLM data for the source contact of the LEFET. (b) I_DV_G measurement for a single-fin device with fin dimensions of 500 nm × 50 µm and LED dimensions of 55 × 55 µm². Current density is calculated using the area of the fin. (c) Linear I_DV_D characteristic (with log-scale in inset) showing reduction in on current of ~ 100x at V_{DS} = 5 V as V_G is reduced from 0 V to -6 V. (d), (e) Qualitative depiction of band diagrams for the device in the on and off states, respectively. With a fixed positive V_{DS}, switching V_G from positive to negative biases modulates electron conduction across the FET channel, and allows voltage to drop across the diode.

The measured electroluminescence (EL) spectra are shown in Figure 3, demonstrating the optical modulation enabled by the FinFET. Figures 3(a) and (b) show the effect of the drain voltage on the emission spectra in linear and log scales for the 500 nm × 50 µm single fin device at a fixed V_G = 4V for V_{DS} between 10V and 13V. Figures 3(c) and (d) demonstrate the desired modulation of the EL spectra through gating of the GaN FinFET.

In summary, we have demonstrated a new technique for achieving monolithic integration of n-FETs and LEDs, using vertical fin-and nanowire-FETs and bottom tunnel junction blue LEDs. This platform allows for strong gate control (~ 5 orders of magnitude on/off for I_D) without limiting the on-wafer LED active area, and does not require regrowth.

Optical switching behavior up to 30 kHz is demonstrated in the first prototype, with room for improvement through use of InGaN heterojunction TJs.

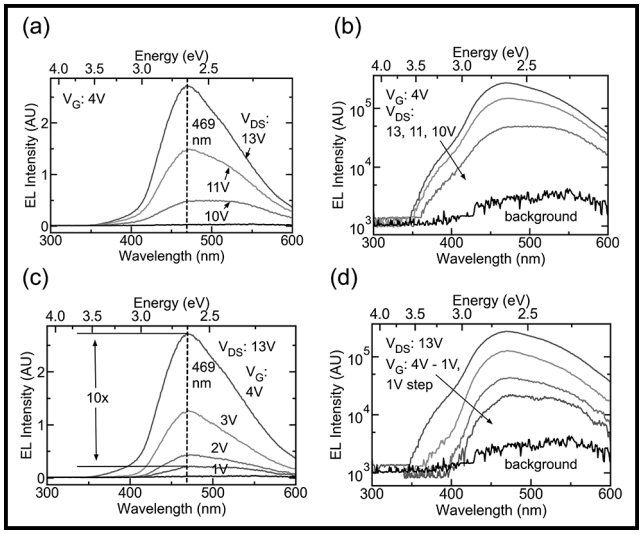

Figure 3: (a), (b) Linear and log scale plots, respectively, of electroluminescence (EL) intensity versus wavelength for a single-fin device, with V_G fixed at +4V. The EL intensity rises as expected with increasing V_{DS} as the level of forward bias across the diode is increased. (c), (d) Linear and log scale plots, respectively, of EL intensity versus wavelength for the same device, with V_{DS} fixed at 13V. A factor of 10 reduction in EL intensity is observed as V_G is decreased from +4V to +1V, demonstrating the gate's ability to limit electron transport into the LED.