Trench Formation and Filling in Silicon Carbide

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Primary CNF Tools Used: Oxford Cobra etcher, PT770 etcher (left chamber), Logitech Orbis CMP

Abstract:

The two main objectives of our time in the CNF was to form deep trenches in silicon carbide and to planarize our polysilicon trench fill material.

Summary of Research:

Our first objective was to etch deep trenches in silicon carbide. In order to achieve this, a patterned metal mask was used since photoresist and oxide have poor etch selectivity relative to SiC in fluorine-based reactive ion etches (RIE).

A metal layer was first deposited on to the bare SiC surface. Photoresist was then applied and lithographically patterned on the metal layer. The trench pattern was then etched into the metal using a chlorine ICP etcher, the PT770, exposing the SiC. Finally, the Oxford Cobra ICP was then used to etch the deep trenches into the exposed SiC using SF_6-based chemistry. The depth of the trench features were measured using the P10 profilometer.

Thick undoped polysilicon was then deposited to fill the deep trenches. In order to remove the polysilicon from non-trench areas and also to planarize the polysilicon over the trenches, chemical-mechanical polishing (CMP) was used.

Additional work still needs to be completed in order to determine whether this process was satisfactory, such as using a scanning electron microscope (SEM) to determine whether the trenches have been completely filled. In addition to this, metal line test features need to be deposited over the array of deep trenches and electrically tested to confirm that they are shorted across the array, verifying that they are not breaking over the trenches.

References:

[1] Bashir, R., and Hebert, F. PLATOP: A novel planarized trench isolation and field oxide formation using poly-silicon. IEEE Electron Device Letters, 17(7), 352-354. doi:10.1109/55.506364 (1996).

[2] Voldman, S. H. The Influence of a Novel Contacted Polysilicon-Filled Deep Trench (DT) Biased Structure and Its Voltage Bias State on CMOS Latchup. 2006 IEEE International Reliability Physics Symposium Proceedings,151-158. doi:10.1109/relphy.2006.251208 (2006).

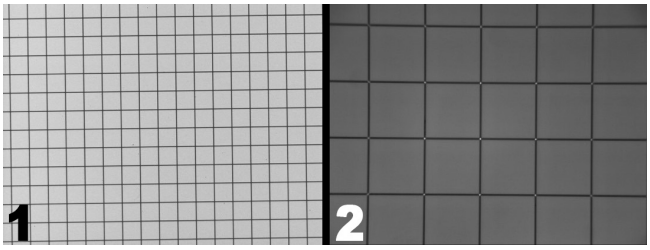

Figure 1, left: Trench features etched into the metal mask. Figure 2, right: Trench features etched into the SiC wafer, no metal mask present.

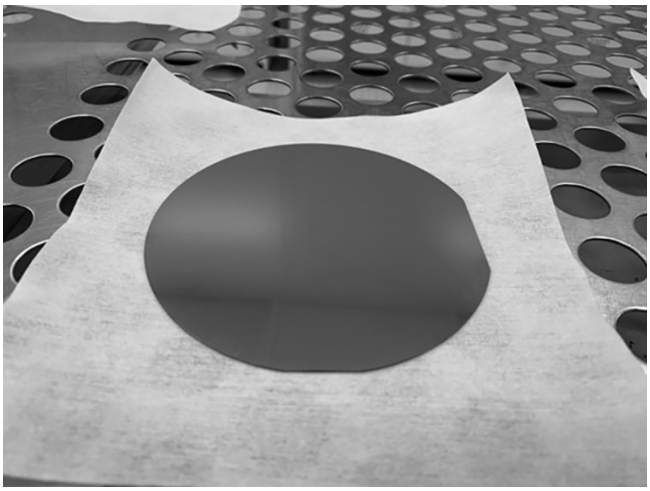

Figure 3: Thick polysilicon on SiC.

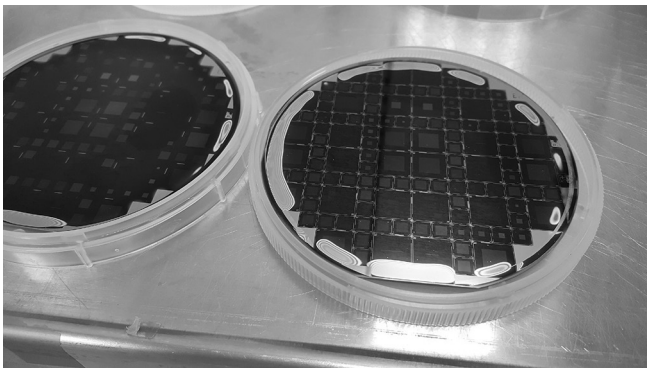

Figure 4: Post-polysilicon CMP.