Nanoscale Periodic Pillar Feature Process Survival

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Primary CNF Tools Used: ASML 300C DUV, GCA 5x Autostep i-line stepper, SEMs

Abstract:

The ASML 300C DUV and GCA 5x Autostep i-line stepper have been used in previous years to produce pillar and hole features with diameters ranging from 232 nm to 446 nm on fused silica and silicon wafers. In recent years hole features have been favored over pillar features because pillars are more likely to break during further front and backside wafer processing. It has been found that pillar features give optical performance up to 3.5 times higher than the hole features in spectral applications. For this reason, pillar feature fabrication with further front and backside wafer processing is explored that gives initial wafer yield of 50% compared to previous hole feature wafer yield of 70%.

Summary of Research:

In previous years a process for patterning nanophotonic pillar and hole structures was developed at CNF that used the ASML 300C DUV stepper as well as the GCA 5x Autostep i-line stepper. These features were etched into the substrate material using the patterned resist as an etch mask. The ASML 300C DUV stepper process has been used to pattern 4-inch borosilicate float glass wafers (“borofloat”), 4-inch fused silica wafers, and 4-inch silicon wafers. Pillar features like those shown in Figure 1 were fabricated with diameters ranging from 232 nm to 816 nm. Hole features like those shown in Figure 2 were fabricated with design diameters ranging from 306 nm to 446 nm. Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. Photonic crystal geometry was examined in the SEM and photonic crystal performance was assessed optically via extraction of waveguided light.

The DUV process previously developed to pattern fused silica wafers with nanophotonic pillar and hole structures was expanded to include automated backside alignment on the ASML 300C DUV stepper. Work done to enable backside alignment was achieved for up to three out of four ASML alignment marks etched into bare fused silica to a depth of 150 nm.

For recent applications, nanophotonic patterning was mainly focused on holes versus pillars because pillars are more likely to break during further processing and wafer handling. In recent years processing steps have been added to the wafer after nanophotonic crystal pattering to include both front and backside aluminum reflector layers as shown in Figure 3. These added layers can be combined with black, opaque absorber layers on both sides to make a monolithic optical bench on a chip ideal for spectrometer applications. These added steps with the dicing of the wafer makes the pillars more exposed to handing that could damage them. It has been found that pillars designed to the same diameter of corresponding holes give spectral responsively between 50% - 350% higher over a range of inputs between 400-1000 nm for designs with a diameter of 446 nm. It is because pillars give such a greater spectral responsively, that they have again been investigated for the monolithic optical bench die design.

This past year, nanophotonic pillar structures with diameters of 612 nm and 816 nm were made in fused silica wafers with the intent of seeing how they would survive further processing to produce the monolithic optical bench die design. These pillars were patterned on fused silica wafers with the ASML 300C DUV and etched into the substrate using the resist as an etch

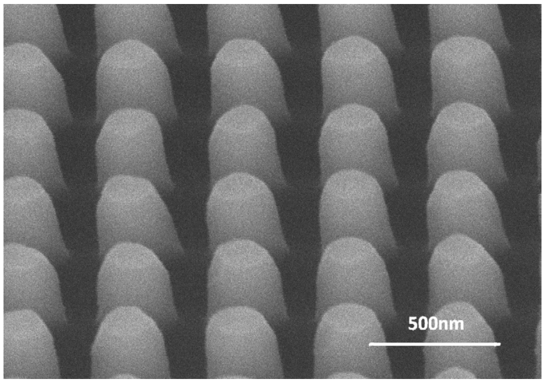

Figure 1: SEM image of photonic crystal pattern, nominally with 270 nm pillar features, fabricated fused silica with process developed with ASML 300C DUV stepper.

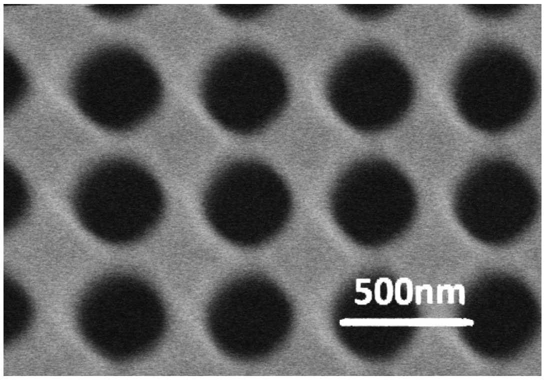

Figure 2: SEM image of photonic crystal pattern, nominally with 306 nm hole features, fabricated in fused silica with a process developed with ASML 300C DUV stepper.

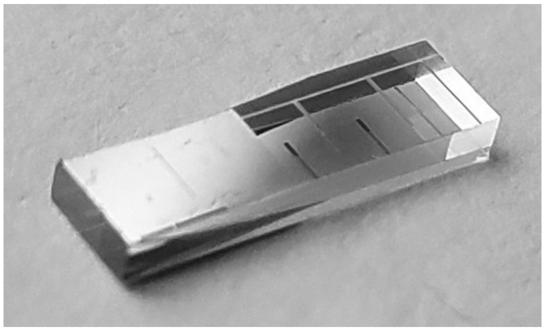

Figure 3: Diced fused silica die with pattered Al reflectors on both sides in addition to the nanophotonic pattern.

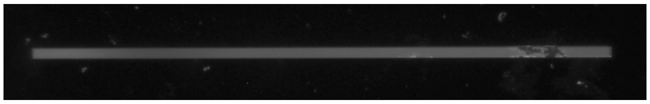

Figure 4: Green (gray) light being scattered through a 306 nm diameter nanophotonic pattern illuminating pillar damage.

mask. The wafers then had aluminum sputtered onto the front and backside, which was patterned via contact lithography plus liftoff and plasma etch respectively. The wafer was then coated with a protective resist layer, diced, and solvent cleaned. The resulting dies where inspected by waveguiding green light into the edge of the die and inspecting the nanophotonic crystal pattern in a microscope to check for defects. Pillar damage from handling is apparent in the example given in Figure 4. Nanophotonic patterns may also be rejected for other kind of defects. An example of a yield for a recent 446 nm diameter hole pattern wafer was 70.5% while the yield for a 612 nm diameter pillar wafer fabricated this year was 50%. Percent yield for a monolithic optical bench die with pillar nanophotonic patterns gives significantly lower yield due to the added aluminum layer processing steps after nanophotonic patterning.

In summary, a process to fabricate nanophotonic pillar structures with diameters of 612 nm and 816 nm has been used to make dies to have further processing including front and backside aluminum patterns. Although pillar features tend to be more fragile when it comes to further wafer processing, these features tend to give higher optical throughput in spectral scattering applications in spectrometer systems. Results of optically imaging of 306 nm diameter patterns with post-processing including front and backside aluminum layers as well as dicing shows a total die yield of 50% for pillars which quite a bit lower than the normal yield for holes which can be around 70%.