High Quality Factor PECVD Si_3N_4 Ring Resonators Compatible with CMOS Process

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Principal Investigator(s): Michal Lipson

User(s): Xingchen Ji, Samantha Roberts

Affiliation(s): Department of Electrical Engineering, Columbia University, New York, NY 10027; School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853

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Contact: ML3745@columbia.edu, xj53@cornell.edu, spr2127@columbia.edu

Primary CNF Tools Used: PECVD, e-beam lithography, Oxford 100 etcher, AJA sputter deposition

Abstract:

We demonstrate high-confinement Si_3N_4 resonators with intrinsic quality factors more than one million using standard PECVD process. We show that by addressing scattering, the loss at 1.6 µm can be as low as 0.4 dB/cm.

Summary of Research:

High quality factor silicon nitride (Si_3N_4) ring resonators are critical for a variety of applications such as low threshold frequency combs [1-3], high precision sensing [4] and optical communications [5]. To date, high quality factor Si_3N_4 ring resonators have been demonstrated almost solely using Si_3N_4 films with high stress, deposited using low-pressure chemical vapor deposition (LPCVD), a high temperature process. Both the high stress of the films and the high temperature process make the fabrication of these devices in a standard foundry challenging.

Plasma-enhanced chemical vapor deposition (PECVD) is a standard, low temperature, commercial process for depositing low stress films. Indeed, achieving low waveguide losses in PECVD Si_3N_4 has been challenging. There have been efforts to reduce losses in PECVD Si_3N_4 films by substituting conventional precursors to deuterated precursors [6], which requires specialized tools and a series of complicated tests. Using standard PECVD, compatible with CMOS processes, the lowest propagation loss reported to date without a high temperature long furnace anneal are 1.6 dB/cm at 1.55 µm and 2.5 dB/cm at 1.6 µm [7,8].

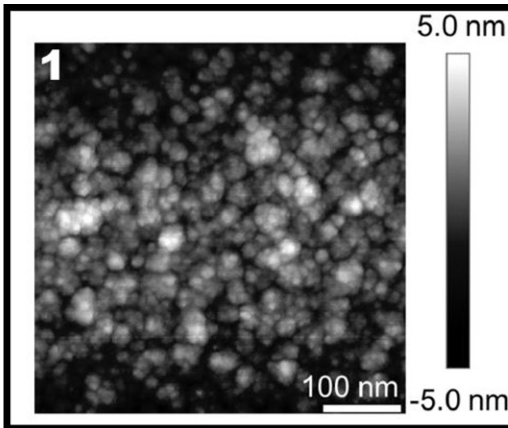
Here we demonstrate Si_3N_4 ring resonators with intrinsic quality factors of more than one million using a standard PECVD process. We show that processes addressing scattering losses such as optimized etch process, chemical-mechanical planarization (CMP) and multipass lithography can lead to quality factors above 700,000. When combined with rapid thermal anneal (RTA) which reduces film absorption loss, quality factors can be more than one million. In contrast to furnace anneal, rapid thermal anneal has been successfully applied in the microelectronics industry. This has particular relevance for CMOS technology, specifically process steps such as implant annealing, oxidation, source and drain contact junctions [9].

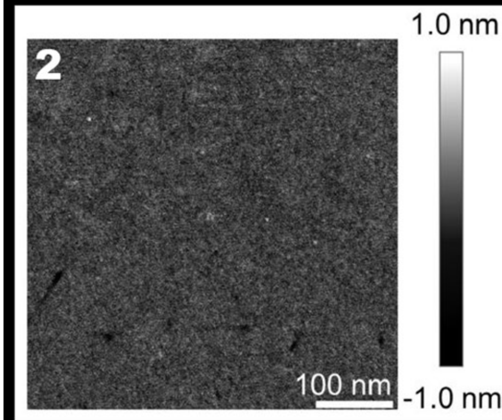
We fabricated our devices on a thermally oxidized 4-inch silicon wafer. Si_3N_4 is deposited using PECVD at 350°C in a single step. CMP, a standard CMOS process, is applied to Si_3N_4 top surface in order to reduce scattering from top surface. The roughness before and after CMP is shown in Figure 1 and Figure 2. The roughness is reduced from 1.36 nm to 0.20 nm. In order to reduce the roughness from the sidewalls, we use a SiO_2 hard mask deposited using PECVD after CMP and use a dry etching process with a higher oxygen flow. This etching process has been shown to reduce substantially the polymerization process during etching and decrease losses [3]. We pattern our devices with electron beam lithography using ma-N 2403 resist and use multipass to further reduce sidewall roughness from lithography. We clad the devices with 2 µm of SiO_2 using PECVD. After cladding, we applied RTA at 800°C for 5 mins to reduce absorption loss.

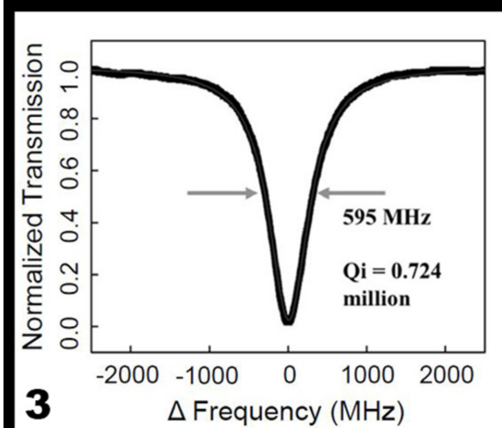
We have achieved an intrinsic quality factor of more than one million using the optimized process. The fabricated devices have radius of 115 µm, height of

730 nm and width of 1500 nm coupled to a waveguide of the same dimensions. These dimensions ensure high confinement. The mode simulation and fabricated devices are shown in Figure 1. In order to test the devices, we launch a tunable laser source, transmitted through a fiber polarization controller, into the inverse nanotaper of our device using a lensed fiber and collect the output of the ring resonator through another inverse nanotaper with a collimating lens. We then monitor the output on a photodetector. Figure 3 shows the measured normalized transmission spectrum before RTA. The measured intrinsic quality factor around 1.6 µm is 724,000, corresponding to a propagation loss of 0.42 dB/cm. Figure 4 shows the measured normalized transmission spectrum after RTA. The measured intrinsic quality factor around 1.6 µm is 1.08 million, corresponding to a propagation loss of 0.28 dB/cm. Therefore, simply by addressing the surface roughness, we are able to achieve propagation loss as low as 0.42 dB/cm. After RTA, we achieve even lower loss of 0.28 dB/cm.

Utilizing CMOS compatible processes including etch optimization, CMP, multipass lithography and RTA, we are able to fabricate low loss waveguides and ring resonators. We have achieved high quality factor more than one million using a standard PECVD process. This work provides a platform for achieving low loss, crack-free Si_3N_4 films, which could greatly benefit applications such as 3D photonic integration, telecommunications and nonlinear processing.







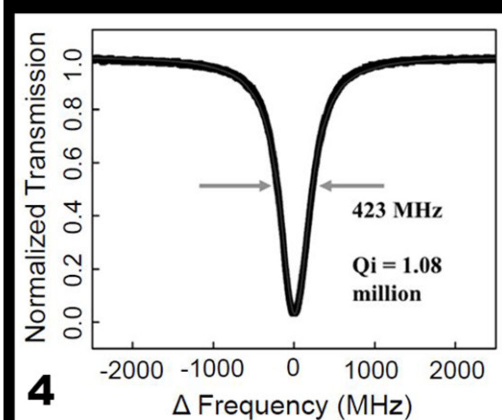


Figure 1: AFM measurement of the top surface of Si_3N_4 before CMP. Roughness of 1.36 nm.

Figure 2: AFM measurement of the top surface of Si_3N_4 after CMP. Roughness of 0.20 nm.

Figure 3: Normalized transmission spectra of the same ring resonator before rapid thermal anneal (RTA). Resonance with 595 MHz linewidth corresponding to an intrinsic Q of 0.72 million.

Figure 4: Normalized transmission spectra of the same ring resonator after rapid thermal anneal (RTA). Resonance with 423 MHz linewidth corresponding to an intrinsic Q of 1.08 million.

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