NanoThermoMechanical Logic Thermal Gates

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Principal Investigator(s): Sidy Ndao

User(s): Ahmed Hamed

Affiliation(s): Mechanical and Materials Engineering, University of Nebraska-Lincoln

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Contact: sndao2@unl.edu, a.hamed@huskers.unl.edu

Primary CNF Tools Used: Heidelberg mask writer DWL2000, ASML 300C DUV, e-beam SC4500 odd evaporator, Oxford PECVD, Oxford 81 etcher, Unaxis 770 etcher, Tencor P7 profilometer

Abstract:

Today's electronics cannot perform in harsh environments (e.g., elevated temperature and ionizing radiation environments) found in many engineering applications. Thermal computing, data processing based on heat instead of electricity, is proposed as a practical solution and opens a new scientific area at the interface between thermal and computational sciences. We designed and modeled thermal AND, OR and NOT logic gates, achieved through the coupling between near-field thermal radiation (NFTR) and MEMS thermal actuation [1]. In the process, we also developed two novel non-linear thermal expansion designs of microstructured chevron beams. Using in-cleanroom standard microfabrication techniques in CNF, we successfully fabricated the designed thermal AND and OR gates.

Summary of Research:

Due to the success and feasibility shown by modeling the designed thermal gates, we were interested in fabricating and characterizing the proposed micro-structured thermal logic gates. In general, the microdevices that intended to be fabricated consist of chevron beams hold suspended plates, all are thermally actuated by platinum microheaters above the silicon microstructures. So, we designed three photolithography masks: platinum microheaters, silicon front side microstructures, and silicon backside etching. The microdevices are fabricated using in-cleanroom standard microfabrication techniques in CNF starting with a four-inch-diameter <100> silicon-over-insulator (SOI) wafer. The SOI wafer consists of a 400 µm thick handle silicon substrate, a 1 µm thick buried silicon dioxide layer, and a 20 µm thick boron-doped silicon device layer.

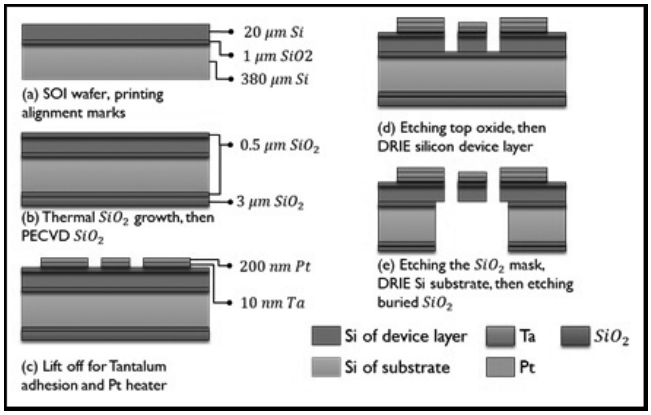

Figure 1: Fabrication steps of the two novel thermal expansion mechanisms (the reducing and the amplification mechanisms).

Figure 1 shows the steps followed through the microfabrication process flow adopted for the thermal gates' fabrication. Following a cleaning step of the wafers, a 0.5 µm thick silicon dioxide film (acts as an electrical insulator) is thermally grown by wet oxidation in a furnace at 1100°C (Figure 1b) on both sides of the wafer. On the substrate's backside, an additional 3 µm thick film of silicon dioxide is deposited via plasma enhanced chemical vapor deposition (tool: Oxford PECVD) to serve as an etching mask in subsequent backside etch steps. The microheaters (200 nm thick platinum and 10 nm thick tantalum as adhesion layer) are formed on top of the device layer using lift-off and e-beam evaporation (tool: SC4500 odd evaporator) as shown in Figure 1c. Following the formation of the microheaters, the suspended structures of the NanoThermoMechanical

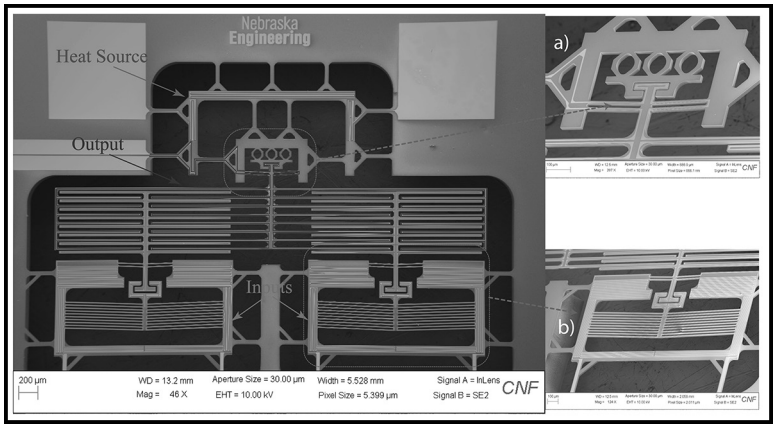

Figure 2: SEM images of the micro-structured thermal logic AND gate including: a) the reducing and b) the amplification mechanism.

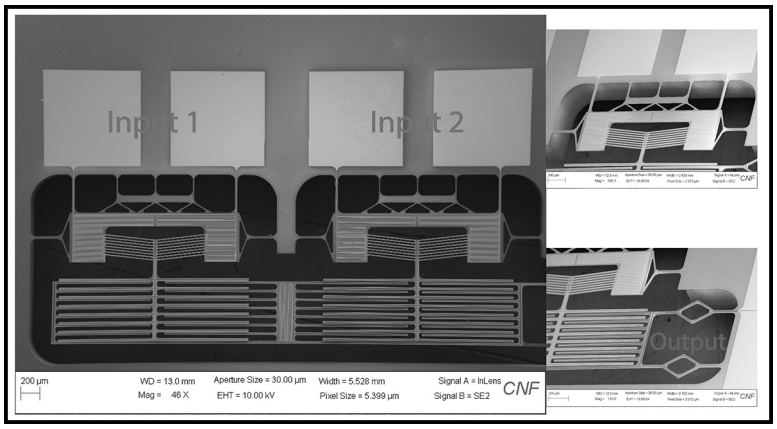

Figure 3: SEM images of the micro-structured thermal logic OR gate including two inputs (chevron beams) and output (fixed terminals).

gate (Figure 1d) were formed through steps of reactive ion etching (tool: Oxford 81 etcher) (to remove the 0.5 µm thick thermal silicon dioxide layer) and deep reactive ion etching of the silicon device layer (tool: Uniaxis 770 etcher). To release the final structures, backside etching (Figure 1e) on the silicon dioxide (tool: Oxford 81 etcher), silicon handle wafer (tool: Uniaxis 770 etcher), and buried oxide were performed (tool: Oxford 81 etcher).

We designed three photolithography masks (Heidelberg mask writer DWL2000): platinum microheaters, silicon front side microstructures, and silicon backside etching. These masks are employed through the microfabrication process flow adopted to fabricate the designed thermal gates. Figures 2 and 3 show the successful micro-fabrication of the thermal AND and OR gates, respectively, including the reducing and the amplification mechanisms for the thermal AND gate.

References:

[1] A. Hamed, M. Elzouka and S. Ndao, "Thermal calculator," International Journal of Heat and Mass Transfer, vol. 134, pp. 359-365, 2019.