Directed Self Assembly of a Stable Radical Polymer

CNF Project Number: 386-90

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Primary Source(s) of Research Funding: Department of Energy Office of Basic Energy Science (Grant DE-SC0014336)

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Primary CNF Tools Used: ASML DUV stepper, Oxford 80+ etcher, Oxford ICP Cobra etcher

Abstract:

We use graphoepitaxy and solvent vapor annealing (SVA) for directed self-assembly of a stable radical block copolymer composed of blocks of poly(2,2,6,6-tetramethylpiperidinyloxy methacrylate) (PTMA) and poly(2,2,2-trifluoroethyl methacrylate) (PTFEMA). We report lamellar and cylindrical morphologies formed by SVA. Silicon substrate is topographically modified to form trenches with two different trench depths. Narrow and deep trenches are shown to assemble the blocks parallel to the trench direction, however with defects. By using a neutral underlayer, we show alignment of the blocks perpendicular to the trench direction. This ordering is further improved by increasing film thickness. Lastly, we study morphologies by using gold sidewalls instead of the silicon sidewalls for chemically heterogeneous graphoepitaxy. We thus demonstrate control over placement of stable radical groups in nanostructures controlled for further electrical characterizations and device fabrication.

Summary of Research:

Introduction. Microphase separation of the block copolymers (BCP) result in the formation of chemically discrete domains ordered in various geometries [1]. Recently, stable radical BCPs have been studied in order to place these stable radical groups in such geometries and study charge transport in these polymers [2,3]. Commonly explored BCP morphologies include the cylindrical (hcp), lamellar, and spherical (bcc) microphases, which can be ordered in the scale of microns. Lamellar morphology BCPs are often utilized in BCP lithography, but their self-assembly typically results in a finger-print like pattern rather than unidirectional order [4]. Directed self-assembly (DSA) has been studied extensively to attain this unidirectional order in lamellar and down-lying cylindrical BCPs. Two common DSA techniques used are graphoepitaxy, which uses topographically patterned substrates and chemoepitaxy, which uses chemically modified substrates [5]. We use graphoepitaxy here to unidirectionally order the two blocks parallel and perpendicular to the trenches using the strategies shown in Figure 1.

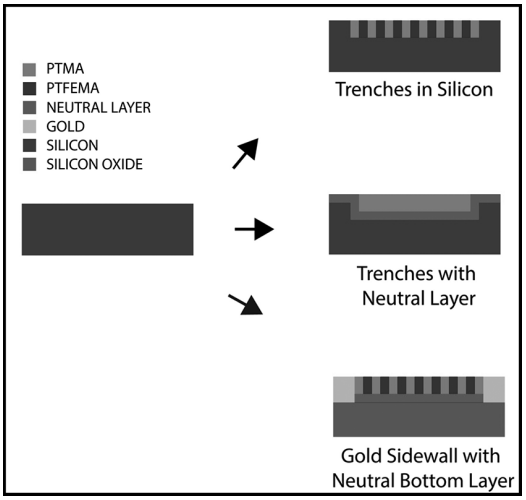

Figure 1: Epitaxial strategies used for direct self-assembly.

Methods. The trenches and gold sidewall are formed by deep UV (DUV) lithography process. Antireflective coating (ARC) DUV42P was first spin-coated followed by the resist UV210. DUV exposures were performed using ASML 300C stepper. The dose was adjusted to achieve the desired trench width at a depth of focus of -0.1 μm. The exposed films were then baked at 130°C for 90s and developed using AZ MIF 726.

The ARC was then etched using Oxford 80+ etcher by using CF_4 and O_2 plasma. The silicon was then etched in Oxford Cobra ICP etcher using an HBr chemistry. The resist was then stripped using Anatech resist strip. Gold sidewalls were prepared using a lift-off process. A 300 nm thick SiO_2 layer was grown on the silicon wafer by PECVD. The line and space patterns were created using the lithography process as mentioned above. ARC layer was then etched as mentioned above. A 5 nm layer of titanium and 100 nm film of gold were deposited on the patterned photoresist using an electron beam evaporator. The metal deposited on the photoresist was lifted off using MICROPOSIT 1165 solution. The BCP had a PTMA block molecular weight of 21,700 g/mol and PTFEMA block molecular weight of 14,300 g/mol having a dispersity of 1.21 when measured by GPC. AFM images were taken using Asylum-MFP3D-Bio-AFM-SPM in tapping mode.

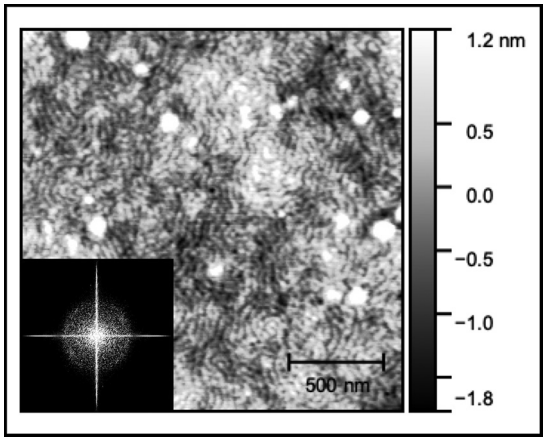

Figure 2: AFM topography image and its 2DFFT (inset) when annealed for three hours.

Results and Discussion:

The block copolymer when annealed using chloroform vapor for three hours exhibited a lamellar morphology as shown in Figure 2. The lamella showed short-range order in a fingerprint-like pattern and thus to enable DSA, we used trenches in the silicon wafer with a trench depth of 120 nm as well as gold sidewalls (100 nm thick). The AFM images are summarized in Figure 3. All films except the one shown in Figure 3e were annealed for six hours. The blocks align parallel to the silicon trenches but with defects as shown in Figure 3a and 3b. The defects exist due to weakly preferential wetting of silicon by PTMA. By grafting a neutral underlayer, we align the blocks perpendicular to the trenches (as shown in Figure 3c and 3d) with an improvement in the alignment with a thicker film. A short-range ordered parallel alignment is also obtained using gold sidewalls due to low vapor pressure annealing for three hours (Figure 3e).

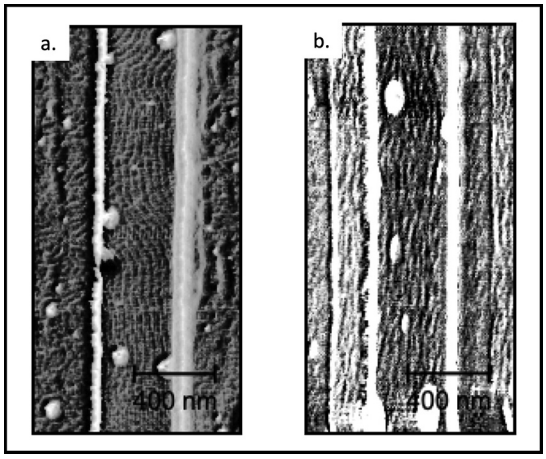

Figure 3: AFM phase images of the thin lm on (a) Si trench (width 480 nm) (b) Si trench (width 448 nm).

Thus, we demonstrate directed self-assembly of the stable radical containing block copolymer in morphologies parallel and perpendicular to the trench direction. This opens up the possibility to elucidate charge transport in stable radical polymers and relate polymer structure to the electrical properties.

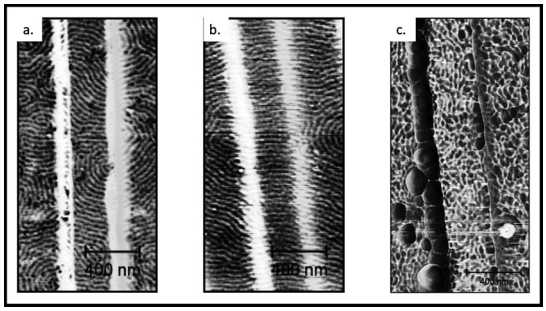

Figure 4: AFM phase images of the thin lm on (a) and (b) Si trench (width 480 nm) and (c) gold sidewall (width 448 nm).

References:

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Nanoscale Periodic Pillar Feature Process Survival

CNF Project Number: 2217-13

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Primary CNF Tools Used: ASML 300C DUV, GCA 5x Autostep i-line stepper, SEMs

Abstract:

The ASML 300C DUV and GCA 5x Autostep i-line stepper have been used in previous years to produce pillar and hole features with diameters ranging from 232 nm to 446 nm on fused silica and silicon wafers. In recent years hole features have been favored over pillar features because pillars are more likely to break during further front and backside wafer processing. It has been found that pillar features give optical performance up to 3.5 times higher than the hole features in spectral applications. For this reason, pillar feature fabrication with further front and backside wafer processing is explored that gives initial wafer yield of 50% compared to previous hole feature wafer yield of 70%.

Summary of Research:

In previous years a process for patterning nanophotonic pillar and hole structures was developed at CNF that used the ASML 300C DUV stepper as well as the GCA 5x Autostep i-line stepper. These features were etched into the substrate material using the patterned resist as an etch mask. The ASML 300C DUV stepper process has been used to pattern 4-inch borosilicate float glass wafers ("borofloat"), 4-inch fused silica wafers, and 4-inch silicon wafers. Pillar features like those shown in Figure 1 were fabricated with diameters ranging from 232 nm to 816 nm. Hole features like those shown in Figure 2 were fabricated with design diameters ranging from 306 nm to 446 nm. Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. Photonic crystal geometry was examined in the SEM and photonic crystal performance was assessed optically via extraction of waveguided light.

The DUV process previously developed to pattern fused silica wafers with nanophotonic pillar and hole structures was expanded to include automated backside alignment on the ASML 300C DUV stepper. Work done to enable backside alignment was achieved for up to three out of four ASML alignment marks etched into bare fused silica to a depth of 150 nm.

For recent applications, nanophotonic patterning was mainly focused on holes versus pillars because pillars are more likely to break during further processing and wafer handling. In recent years processing steps have been added to the wafer after nanophotonic crystal pattering to include both front and backside aluminum reflector layers as shown in Figure 3. These added layers can be combined with black, opaque absorber layers on both sides to make a monolithic optical bench on a chip ideal for spectrometer applications. These added steps with the dicing of the wafer makes the pillars more exposed to handing that could damage them. It has been found that pillars designed to the same diameter of corresponding holes give spectral responsively between 50% - 350% higher over a range of inputs between 400-1000 nm for designs with a diameter of 446 nm. It is because pillars give such a greater spectral responsively, that they have again been investigated for the monolithic optical bench die design.

This past year, nanophotonic pillar structures with diameters of 612 nm and 816 nm were made in fused silica wafers with the intent of seeing how they would survive further processing to produce the monolithic optical bench die design. These pillars were patterned on fused silica wafers with the ASML 300C DUV and etched into the substrate using the resist as an etch

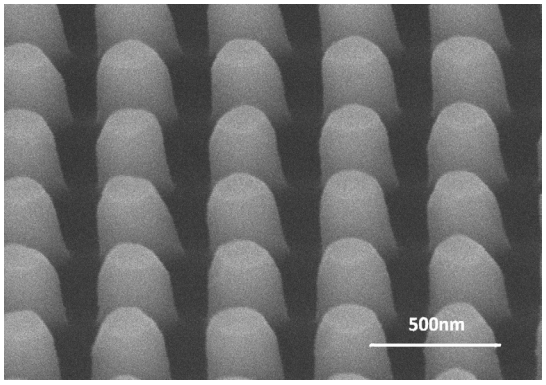

Figure 1: SEM image of photonic crystal pattern, nominally with 270 nm pillar features, fabricated fused silica with process developed with ASML 300C DUV stepper.

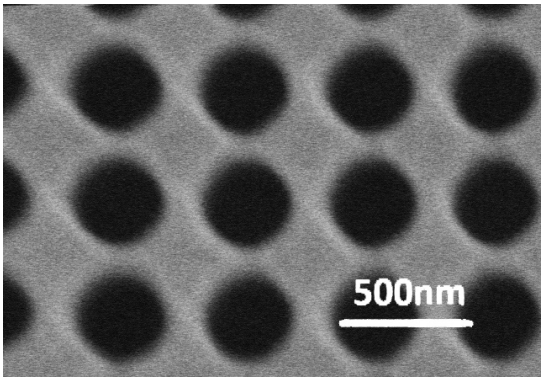

Figure 2: SEM image of photonic crystal pattern, nominally with 306 nm hole features, fabricated in fused silica with a process developed with ASML 300C DUV stepper.

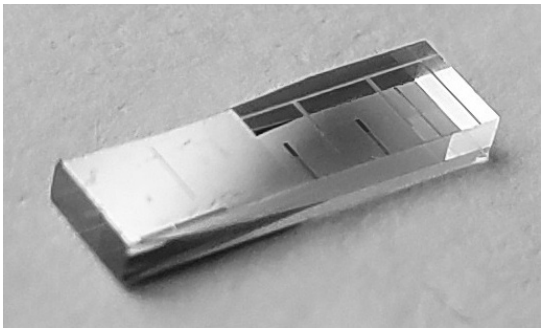

Figure 3: Diced fused silica die with pattered Al reflectors on both sides in addition to the nanophotonic pattern.

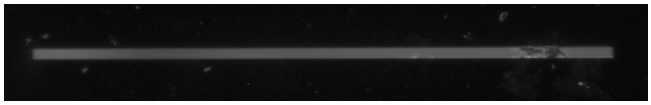

Figure 4: Green (gray) light being scattered through a 306 nm diameter nanophotonic pattern illuminating pillar damage.

mask. The wafers then had aluminum sputtered onto the front and backside, which was patterned via contact lithography plus liftoff and plasma etch respectively. The wafer was then coated with a protective resist layer, diced, and solvent cleaned. The resulting dies where inspected by waveguiding green light into the edge of the die and inspecting the nanophotonic crystal pattern in a microscope to check for defects. Pillar damage from handling is apparent in the example given in Figure 4. Nanophotonic patterns may also be rejected for other kind of defects. An example of a yield for a recent 446 nm diameter hole pattern wafer was 70.5% while the yield for a 612 nm diameter pillar wafer fabricated this year was 50%. Percent yield for a monolithic optical bench die with pillar nanophotonic patterns gives significantly lower yield due to the added aluminum layer processing steps after nanophotonic patterning.

In summary, a process to fabricate nanophotonic pillar structures with diameters of 612 nm and 816 nm has been used to make dies to have further processing including front and backside aluminum patterns. Although pillar features tend to be more fragile when it comes to further wafer processing, these features tend to give higher optical throughput in spectral scattering applications in spectrometer systems. Results of optically imaging of 306 nm diameter patterns with post-processing including front and backside aluminum layers as well as dicing shows a total die yield of 50% for pillars which quite a bit lower than the normal yield for holes which can be around 70%.

Size Characterization of Plasma Membrane Vesicles, Virus Particles, and Synthetic Vesicles

CNF Project Number: 2575-17

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Primary CNF Tools Used: Nanosight

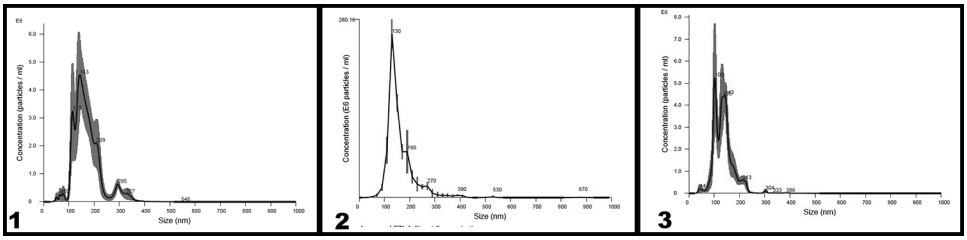

Figure 1, left: Concentration vs size (nm) distribution plot for pseudotyped virus particles. Figure 2, center: Concentration vs size (nm) distribution plot for plasma membrane vesicles. Figure 3, right: Concentration vs size (nm) distribution plot for synthetic vesicles.

Abstract:

Nanosight was used to determine the concentration and size distribution of various biologically relevant particles, including viruses and plasma membrane vesicles.

Summary of Research:

Our research investigates interactions of biologically relevant particles (viruses, microvesicles, plasma membrane vesicles) on a supported lipid bilayer and with synthetic vesicles.

Most of the particles used are generated in-house and as such, it is important to characterize them (diameter, size distribution, concentration of particles) to ensure that we are using the similar quality and concentration of particles across various experiments for consistency. The concentration is especially important as too much or too little of the plasma membrane vesicles used to form the supported lipid bilayer will influence the bilayer's diffusivity and patchiness and varying concentration of viral particles may impact fluorescent dye incorporation.

Typical sizes of viruses, plasma membranes vesicles, and synthetic vesicles that we use range from 100-200 nm and typical values of concentration are on the order of 10^8 particles/mL for plasma membrane particles, 10^{10} particles/mL for viruses and 10^{12} particles/mL for synthetic vesicles.

Nanoslit Silicon Nitride Fabrication for Virus Filtration

CNF Project Number: 2660-18
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User(s): Joshua Miller

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Primary Source(s) of Research Funding: National Institutes of Health
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Primary CNF Tools Used: ASML 300C DUV stepper, SÜSS MicroTec Gamma Cluster Tool

Abstract:

Existing and widely used 0.2/0.22 µm polymer filters are not well-suited for sterilizing larger non-protein biological therapeutics during their production, as these filters entrap these molecules, thus contributing to significant yield loss. Here, we report on the fabrication of nanoslit silicon nitride (NSN) membranes with isoporous sub-0.2 µm rectangular "pores" for addressing the need for improved biological therapeutic sterile filtration. For this project, we used CNF's SÜSS MicroTec Gamma Cluster Tool and the ASML 300C DUV 4x reduction stepper, as well as various tools at Rochester Institute of Technology (RIT) Semiconductor and Microsystems Fabrication Laboratory (SMFL) to produce novel NSN sterile filters.

Summary of Research:

SiMPore produces a variety of suspended thin film membranes both porous and non-porous. For this project, the capability of the ASML 300C was explored for the fabrication of 200 nm wide slits. Capability for patterning this feature size is not available at SiMPore's home cleanroom (RIT SMFL). Prior to this project, SiMPore offered nanomembrane filters with either pore sizes ranging from 500 nm - 8 µm or sub-70 nm by way of SiMPore's NanoPorous silicon nitride (NPN) membranes, but the range in-between has been missing from SiMPore's offerings.

In this work, the SÜSS MicroTec was used to spin on 60 nm DUV 42P anti-reflective coating (ARC), then approximately 500 nm UV210 positive photoresist over 200 nm low stress silicon nitride on 150 mm diameter, 310 µm thick double side polished (DSP) wafers. The mask designed for this project had four iterations: 1:1 pitch 200 nm slits, 1:2 pitch 200 nm slits, 1:3 pitch 200 nm slits, and finally 1:2 pitch 150 nm slits. These sizes allowed exploration of strength vs. fluency as well as the ability to make slightly different sizes via over exposure, if desired. The ASML 300C was then used to expose each pattern by Focus Exposure Matrix (FEM). The resultant FEM features were then etched into the nitride, the feature sizes were measured with a Zeiss Auriga scanning electron microscope, and the optimal conditions were extrapolated. Once the conditions were selected, additional wafers were coated, exposed continuously across the entire frontside of the wafer, developed at CNF, and then taken back to RIT SMFL for further processing.

At RIT SMFL, the ARC was removed by a low power reactive ion etch (RIE) in a Trion and then the 200 nm SiN was etched via plasma etch in a LAM 490. The wafers were then stripped of the residual resist using Piranha and protected on the frontside with a silicon oxide derived from tetraethylorthosilicate (TEOS) using an AMAT Precision 5000 system. The wafers were then flipped to expose a backside pattern, etched in a similar fashion as the slit features, and then stripped. This backside pattern defined SepCon membrane chips with four (4) 0.3 mm by 3 mm porous membranes and a total chip size of 5.4 mm by 5.4 mm. Finally, the silicon wafers were bulk-etched from the backside with a crystallographic etchant and the frontside protective oxide was removed with buffered oxide etchant (BOE). See Figure 1 for process flow, and Figure 2 for scanning transmission electron microscope (STEM) images of the nanoslits.

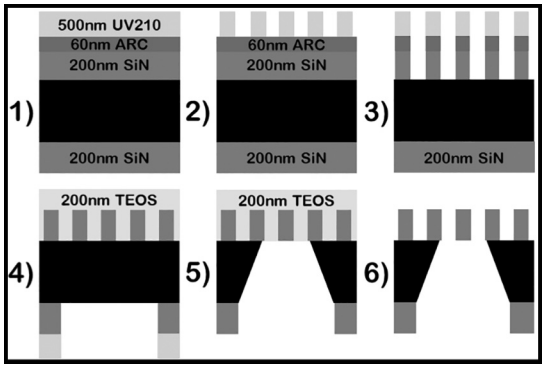

Figure 1: Process flow for NSN chips; 1) ARC plus Resist application, 2) Exposure with ASML 300C, 3) RIE of ARC and nitride to form nanoslits, 4) Frontside protection with TEOS and backside patterning, 5) Backside crystallographic etch to free-stand membranes, 6) Final porous membrane chips.

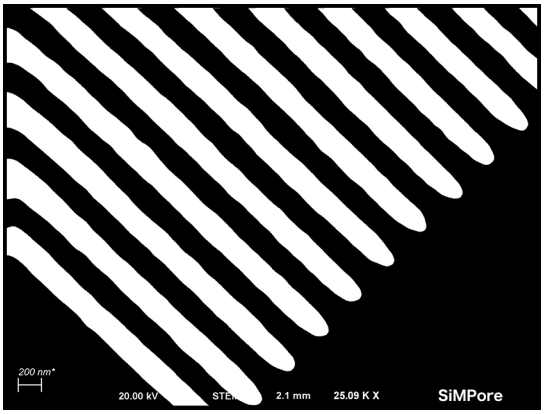

Figure 2: 25kX magnification STEM of 200 nm slits with 1:1 pitch.

One of the challenges faced in this work was the limited depth of focus (DOF) for these feature sizes. 200 nm slits are the practical limit of the 248 nm DUV light source on the ASML 300C. Due to this, we are operating at the maximum NA and Sigma, which further narrows the DOF. Another difficulty we experienced stemmed from the thinness of our wafers. The 310 µm thick wafers used for this process have considerable flex when held by a vacuum chuck (as the ASML does during exposures). The result of this is a significant loss of real estate on the final wafer, as the flexed portions of the wafer were out of focus and their features under-exposed. To combat this, our current tests use 675 µm thick wafers, and following frontside patterning, will be backside-ground and re-polished to 310 µm for subsequent bulk-etching. The resulting patterned features are significantly more uniform across the entire surface of the wafer. While there were still some aberrations; the use of ultra-flat wafers in the future may be necessary for complete and uniform exposures across a full 150 mm wafer.

In the next year, we will continue to pursue complete uniformity across these wafers, trying with tighter specified flatness, with the goal of fully useable wafers. Additionally, we will attempt using the same mask for slightly larger features to see if that will help alleviate some of the DOF issue. Our preliminary evidence suggests the 150 nm slits, when over exposed produce viable 200 nm slits at roughly 1:1 pitch.