Power Electronic Devices Based on Ga_2O_3

CNF Project Number: 2307-14

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Primary Source(s) of Research Funding: NSF DMREF Program under Grant 1534303 AFOSR under Grants FA9550-17-1-0048, FA9550-18-1-0529 and FA9550-18-1-0479

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Primary CNF Tools Used: Oxford PECVD and ALD, odd-even hour evaporation, AJA sputtering tool, PT-770 etcher

Abstract:

Gallium(III) trioxide (Ga_2O_3) is an ultra-wide bandgap semiconductor material with excellent breakdown electric field and the availability of melt-grown substrates, thus very promising for power electronic devices. Employing a vertical device topology, we have been able to successfully demonstrate Ga_2O_3 power diodes and transistors with excellent device performance, including a breakdown voltage exceeding 2 kV, as well as state-of-the-art on-state performance. Through electrostatic engineering and process optimization, we are pushing toward the limit of this material, which could surpass the performance of current power devices based on SiC and GaN.

Summary of Research:

β-Ga_2O_3 has attracted considerable interests as a promising wide-bandgap semiconductor material for power devices. Aside from the availability of melt-grown substrates, the sizable bandgap value of 4.5-4.7 eV allows for a large critical electric field exceeding 5 MV/cm as observed experimentally. Aided by the excellent field strength, high breakdown voltage exceeding 1 kV has been demonstrated in both diodes and transistors. In addition, a Baliga's figure-of-merit (BFOM) of around 0.5 GW/cm^2 has been achieved in both lateral and vertical Schottky barrier diodes (SBDs), which already exceeded the unipolar limit of Si.

Vertical power devices can provide higher current density than the lateral counterparts. With the incorporation of fin-channels, vertical enhancement-mode Ga_2O_3 transistors with good gate-control [1,2] as well as vertical Ga_2O_3 trench Schottky barrier diodes with reduced reverse leakage current [3,4] have been realized by our group.

The fabrication process for the Ga_2O_3 trench Schottky barrier diodes is as follows: First, reactive ion etch (RIE) based on BCl_3 and Ar was performed on the backside of the wafer to facilitate ohmic contact using the PT-770 etcher; After that, Ti (50 nm)/Au (125 nm) was evaporated on the backside as the cathode contact followed by a rapid thermal anneal (RTA) for 1 min under N_2 ambient; Next, Ni/Pt were deposited and patterned by a lift-off process on the top surface, serving as the Schottky contact as well as the hard mask for the subsequent etching for trench formation; Trenches with a depth of 1-2 μm were etched using RIE; Subsequently, a 100-nm Al_2O_3 dielectric layer was deposited by atomic layer deposition (ALD) using the Oxford ALD tool; Next, the dielectric was opened by dry etching to expose the Ni/Pt Schottky contact, followed by a deposition of Cr/Pt over the sidewall by sputtering using the AJA sputtering tool.

The fabrication process for the Ga_2O_3 vertical fin transistors is as follows: Si ion implantation and activation was performed in the top 50 nm of the drift layer; Pt metal masks were then patterned by electron beam lithography and deposited by electron beam evaporation on the sample surface to define position and size of the FET channels; Vertical Fin-channels were etched in the PT-770 etcher with a target width/height of 0.3/1.0 μm, respectively; Then, a 30 nm Al_2O_3 was deposited by atomic layer deposition (ALD) as the gate dielectric, followed by a 50 nm thick Cr sputtered as the gate metal; A photoresist planarization process was used

to selectively etch away the gate metal/dielectric on top of the n^+-Ga_2O_3 source; Then, a 200 nm SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) using the Oxford PECVD tool and a second planarization process was used to etch away the SiO_2 on top of the n^+ source; Finally, source ohmic contacts were formed by depositing Ti/Al/Pt, and device isolation was realized by etching away SiO_2 and Cr between active devices.

The trench Schottky barrier diodes have a specific on-resistance of 10^{-11} mW·cm^2. In comparison with the regular Schottky barrier diode, the trench diodes possess not only a lower leakage current, but also a higher breakdown voltage. In a number of 1-μm and 2-μm channel devices, the leakage current is below our measurement noise floor (1 μA/cm^2) even at a voltage of more than 2 kV. The reduction of the leakage current directly translates to the reduction of the off-state power loss.

All the vertical Ga_2O_3 MISFETs exhibit normally-off operation. The drain current reaches ~ 300-500 A/cm^2 with an associated differential on-resistance of ~ 13-18 mW·cm^2 in devices with a channel width of 300 nm. In devices with a channel width of 400 nm, the current density reaches over 1000 A/cm^2.

At off state, the device records very low drain and gate leakage currents. The 3-terminal breakdown voltage is over 1 kV. The breakdown is identified to be due to field crowding at the device periphery. With improved edge termination designs, the breakdown voltage is expected to be much higher.

In summary, we have demonstrated kV-class Ga_2O_3 power diodes and transistors. These initial device results showed a great potential of Ga_2O_3 as a promising material for power electronics applications.

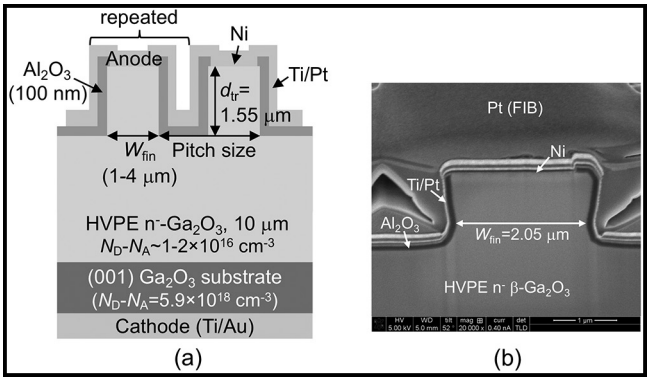

Figure 1: Schematic and SEM cross-section of the Ga_2O_3 trench Schottky barrier diodes.

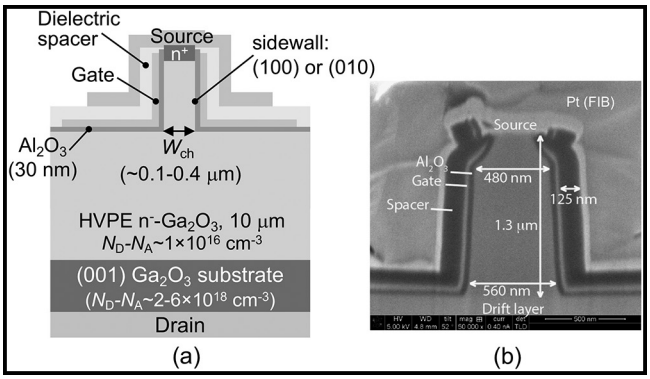

Figure 2: Schematic and SEM cross-section of the Ga_2O_3 vertical fin transistors.

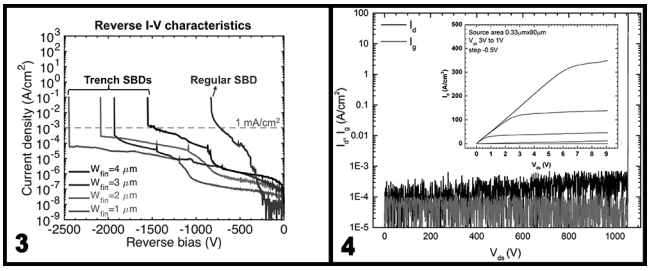

Figure 3, left: Reverse I-V characteristics of the Ga_2O_3 trench Schottky barrier diodes. Figure 4, right: Output I-V characteristics (inset) and reverse I-V characteristics of the Ga_2O_3 vertical fin transistors.

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WSe_2 RF MOSFETs and CMOS Integration

CNF Project Number: 2509-16

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Affiliation(s): Department of Electrical and Computer Engineering, Lehigh University

Primary Source(s) of Research Funding: This work was supported in part by the U.S. Office of Naval Research under Grant N00014-14-1-0653 and the Air Force Office of Scientific Research and the National Science Foundation EFRI 2-DARE Grant No. 1433459-EFMA

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Primary CNF Tools Used: ABM contact aligner, Autostep I-line stepper, PT720-740 etcher, SC4500 odd-hour evaporator, P10 profilometer

Abstract:

We've demonstrated that it is practical and promising to integrate TMDs or other 2D materials into current CMOS process based on large-scale transferred CVD MoS_2, dispensed liquid-exfoliated MoS_2, and temperature assisted converted $PtSe_2$ [1-4]. Of all two-dimensional (2D) atomic-layered materials, WSe_2 is particularly attractive for electronic applications because it has a sizable bandgap, a high carrier mobility, and can be grown on large scale by chemical vapor deposition (CVD). Additionally, both p-type and n-type conductions have been demonstrated, making it possible to realize complimentary logic in WSe_2. In the present experiment, CVD-grown millimeter-sized WSe_2 flakes were etchant-free transferred onto Al gates covered by 30-nm-thick Al_2O_3 gate insulation. With Al_2O_3 passivation, the fabricated WSe_2 MOSFETs were found stable for more than five months. The Al_2O_3 passivation had the additional benefit of enhancing the current capacity of the MOSFETs by two orders of magnitude. Temperature-dependent small-signal microwave measurements showed that both the forward current-gain cut-off frequency (f_T, Figure 1a) and the maximum frequency of oscillation (f_{MAX}, Figure 1b) of the MOSFETs tend to peak near room temperature, with f_T ~ 600 MHz and f_{MAX} ~ 2 GHz (Figure 1c) [5].

Summary of Research:

Fabrication. The main difference of the fabrication between this work and [1] is in the material preparation part. In this work, multilayer tungsten diselenide (WSe_2) films were synthesized on c-plane sapphire substrate through a multi-step gas source chemical vapor deposition (CVD) process [6]. After CVD growth, the film was transferred onto the target chip by an etchant-free transfer method [7].

Passivation Result. The transfer curves of the device at row 5 column 8 (Device 0508) before and after passivation are shown in Figure 2(a). With passivation, the transfer curve, under drain-source bias (V_{DS}) of 1 V, shows current capacity increased by more than two orders of magnitude from ~ 1 nA/μm to ~ 200 nA/μm. Although the on/off ratio decreased, the resulting transconductance still increased from ~ 0.5 nS/μm to ~ 30 nS/μm. In five months, the transfer characteristics did not show noticeable change compared with the characteristics directly after passivation.

DC & RF Thermal Dependence. Figure 2(b) and (c) shows the output and transfer characteristics under different temperature ranging from 223 K to 373 K, of the device at row 3 column 10 (Device 0310). From Figure 2(b), higher temperature leads to saturation at lower V_{DS} because the increasing phonon scattering lowered the mobility and saturation velocity of the electrons. The drain current decreased with increasing temperature under the same biases. The output curves also indicated that when V_{DS} < 1 V, the device characteristics were dominated by large resistances, which were probably the contact resistances at drain and source. From Figure 2(c), with increasing temperature, the hysteresis first increased and then decreased until at 373 K, the device showed p-type conduction, which suggested that temperature as high as 373 K could effectively anneal the sample and even change the conduction carrier type.

Figure 1(a) and (b) show the current gain and power gain of Device 0310 separately after de-embedding under different temperature. The f_T and f_{MAX} peak near room temperature (Figure 1c). The reason f_T and f_{MAX} peak near room temperature is probably due to competing temperature effects. For example, contact resistance, carrier mobility, and saturation voltage all decrease with increasing temperature. These competing effects are being characterized and will be incorporated into a device model to evaluate their combined effect.

Future Direction. First, the uniformity of device performances across the same chip based on single CVD film can be improved. Other than film uniformity itself, direct growth should also help as in the transfer process, the stress introduced by wrinkles during transfer is different at different locations. Second, better interface can be formed if the process can be done in connected ultra-high vacuum (UHV) chambers. This can help to rule out the ambient environment effects in the analysis and make results more reproducible. Third, hexagonal boron nitride can be used as both dielectric and passivation buffer layer to offer better interface and possibly better thermal stability. Finally, introducing contact bias and gate-length dependence study to truly understand the 2D channel.

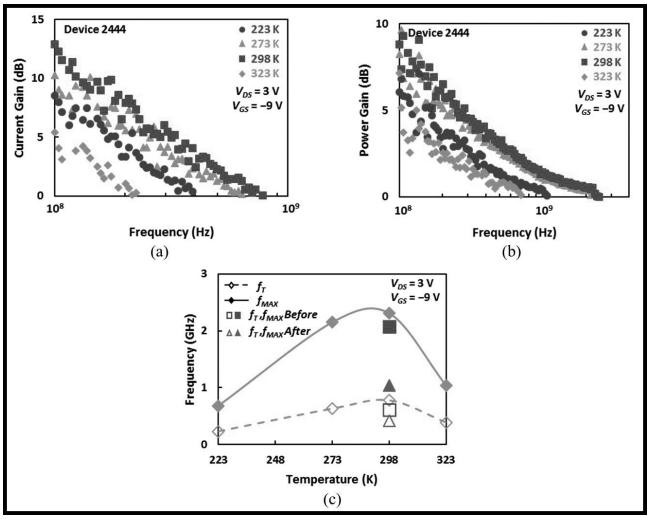

Figure 1: Temperature dependence of de-embedded small-signal (a) current gain, (b) power gain, and (c) cutoff frequencies. (Find full color on pages xiv-xv.)

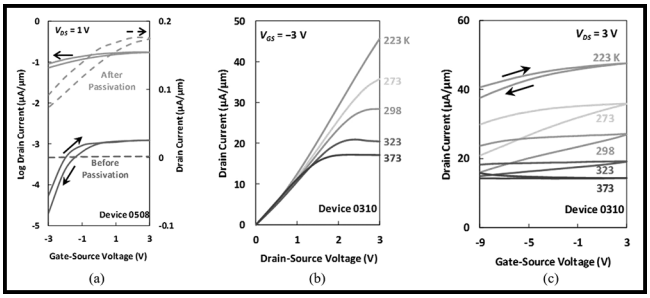

Figure 2: (a) Drain current under different gate-source voltages in log and linear scale, V_{DS} = 1 V, (b) output curves (V_{GS} = -3 V) and (c) transfer curves (V_{DS} = 3 V) of device 0310 under different temperatures (223, 273, 298, 323, 373 K).

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Fully Transparent Oxide Thin-Film Transistor with Record Current and On/Off Ratio

CNF Project Number: 2543-17

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User(s): Jisung Park

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Primary Source(s) of Research Funding: Air Force Office of Scientific Research - DOD

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Primary CNF Tools Used: PT720/740, PVD75 sputter deposition, Oxford ALD FlexAL, Autostep i-line stepper

Abstract:

Here we report making a fully depleted micrometer-scale barium tin oxide ($BaSnO_3$)-based fully transparent TFT that sources over 1.6 mA/μm of current with an on/off ratio over 10^8 and a peak mobility of 68 $cm^2V^{-1}s^{-1}$ at room temperature. Further scaling of these TFTs is expected to provide performance rivaling today's most advanced and scaled transistors. Our results demonstrate the tremendous potential of $BaSnO_3$ for the future of transparent oxide electronics.

Summary of Research:

A fully transparent oxide TFT based on $BaSnO_3$ has been fabricated with record drain current and on/off current ratio. This breakthrough is made possible by (1) high mobility bare films in combination with (2) the development of a micrometer-scale etching method for $BaSnO_3$ that preserves the surface roughness, conductivity, resistivity and mobility of $BaSnO_3$ films. These results demonstrate the tremendous potential of $BaSnO_3$ for the future of transparent electronics.

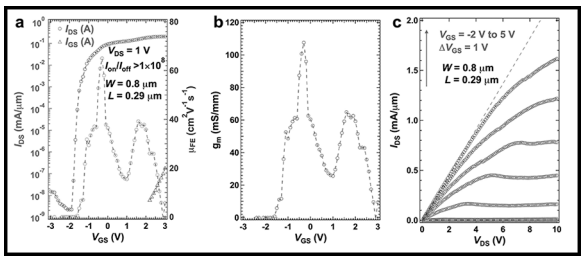

Figure 1: Thin-film transistor based on La-$BaSnO_3$. a, The transfer characteristic of the TFT in the linear region (V_{DS} = 1V) and the transconductance. The peak field-effect mobility is 68 $cm^2V^{-1}s^{-1}$ and the on-off ratio is over 10^8. The subthreshold swing is 0.1 V dec^{-1}. b, Transconductance of the device at V_{DS} = 1V. The maximum transconductance is 10^7 mS/mm. c, The output characteristic of the device at V_{GS} = -2, -1, 0, 1, 2, 3, 4, 5 V. The maximum drain current exceeds 1.6 mA/μm.

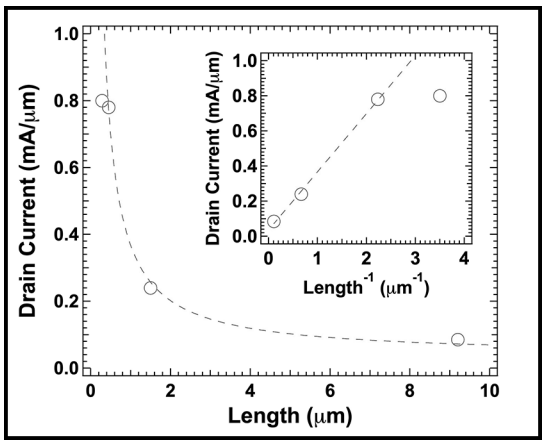

Figure 2: Drain current dependence on channel length (L) when V_{GS} = 3 V and V_{DS} = 10 V. The drain current (I_{DS}) is inversely proportional to the overall channel length except at the shortest channel length, showing little degradation with respect to device scaling. The deviation from linear behaviour in the inset at the shortest channel length is consistent with a velocity saturation effect: the degradation of the mobility and thus the drain current as the carrier velocity is limited by increased scattering rate at the high electric field at short channel length.

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Injectable Micro-Scale Opto-Electrically Transduced Electrodes (iMOTEs)

CNF Project Number: 2578-17

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User(s): Sunwoo Lee, Alejandro J. Cortese

Affiliation(s): Electrical and Computer Engineering, Cornell University

Primary Source(s) of Research Funding: National Institute of Health

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Primary CNF Tools Used: ABM contact aligner, AJA sputter, Westbond 7400A ultrasonic wire bonder, Oxford 100 / 81 / 82, Unaxis deep Si etcher, Oxford PECVD, Oxford ALD, Anatech, P7 profilometer, ZEISS Ultra and Supra SEMs

Abstract:

Recording neural activity in live animals *in vivo* poses several challenges. Electrical techniques typically require electrodes to be tethered to the outside world directly via a wire, or indirectly via an RF Coil [1], which is much larger than the electrodes themselves. Tethered implants result in residual motion between neurons and electrodes as the brain moves, and limits our ability to measure from peripheral nerves in moving animals, especially in smaller organisms such as zebra fish or fruit flies. On the other hand, optical techniques, which are becoming increasingly powerful, are nonetheless often limited to subsets of neurons in any given organism, impeded by scattering of the excitation light and emitted fluorescence, and limited to low temporal resolution [2]. Here we present the electronics for an untethered electrode unit, powered by, and communicating through a microscale optical interface, combining many benefits of optical techniques with high temporal-resolution recording of electrical signals, named Injectable Micro-scale Opto-electrically Transduced Electrodes (iMOTEs).

Summary of Research:

Our fabrication starts with a 5mm × 5mm, conventional 180 nm CMOS die, which contains the electronics for signal amplification, encoding, and transmission. The CMOS die is then integrated with AlGaAs diode, which acts as a photo-voltaic (PV) as well as light emitting diode (LED), hence the diode is abbreviated as PVLED. The PVLED provides an optical link that powers the electronics and transmits encoded signals in optical pulses. The MOTE utilizes pulse position modulation (PPM) for signal encoding for its high information-per-photon efficiency, where the spacing between the output pulses is proportional to the measured electric field of neuronal signals across the measurement electrodes.

Figure 1 depicts a conceptual deployment and simplified schematic of described iMOTE [3].

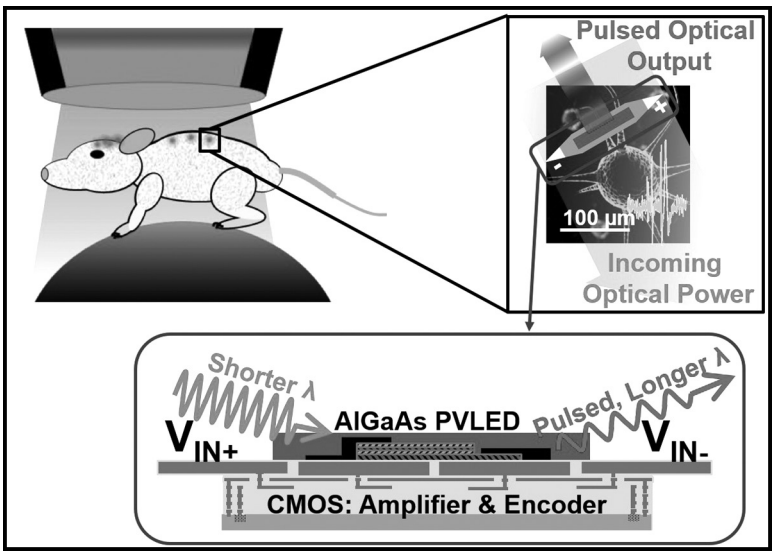

Figure 1: An envisioned implementation of the iMOTE along with a simplified system description.

The AlGaAs diodes are first fabricated on a sapphire wafer, to be later released from the sapphire substrate with a sacrificial poly(methyl methacrylate) (PMMA) polymer. Once the PMMA-coated AlGaAs diodes are transferred onto the CMOS die, the Oxford 81 plasma etcher is used to remove the sacrificial PMMA, leaving only the diodes array intact on the CMOS die. To establish the electrical contact between the PVLED and CMOS, we have used the CNF ABM contact aligner for photolithography with AZ nLof2020 UV photoresist for efficient lift-off process that ensues after metal deposition. After the contact fabrication, the contacts of CMOS and PVLED are connected via similar photo-lithography process, and to maximize the conformality of the metal routing, we employ AJA sputter.

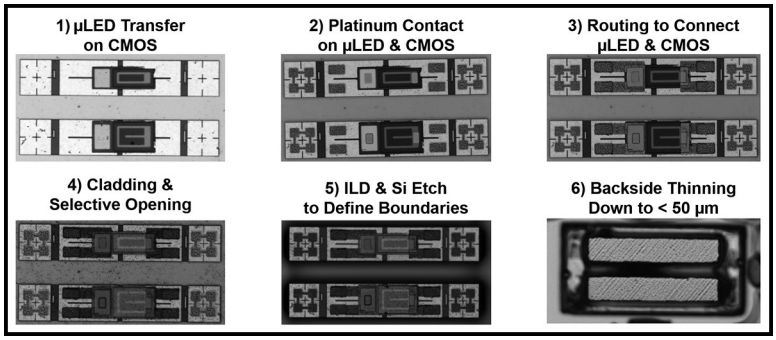

Figure 2: Fabrication flow of iMOTE integration where AlGaAs PVLED is integrated on CMOS. 1) Micro-scale PVLED is transferred on CMOS, 2) platinum contacts fabricated on both PVLED and CMOS, 3) platinum routing is added to connect the contacts made in 2), 4) iMOTEs are passivated with SiO_2 and Si_3N_4 except for its input electrodes openings, 5) using dielectric etching and deep silicon etching, iMOTEs are 'cookie-cut', 6) backside etching allows thinning-down below 50 µm.

Following the routing step, each iMOTE is encapsulated using Oxford ALD and PECVD for SiO_2 and Si_3N_4 deposition, followed by dielectric etching using Oxford 100 and Unaxis deep reactive ion etch (DRIE) for release. Figure 2 described the fabrication sequence described herein.

It should be noted that before making much changes are made in fabrication flow, to confirm the functionality of each module (CMOS and the diode), we use Westbond 7400A ultrasonic wire bonder for board-level test. ZEISS Ultra and Supra scanning electron microscopes (SEMs) are also used to inspect the fabricated iMOTE for debugging purposes.

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Trench Formation and Filling in Silicon Carbide

CNF Project Number: 2755-18
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User(s)): Aysanew Abate

Affiliation(s): CoolCAD Electronics, LLC
Primary Source(s) of Research Funding: National Aeronautics and Space Administration (NASA)
Contact: zeynep.dilli@coolcadelectronics.com, aysanew.abate@coolcadelectronics.com
Primary CNF Tools Used: Oxford Cobra etcher, PT770 etcher (left chamber), Logitech Orbis CMP

Abstract:

The two main objectives of our time in the CNF was to form deep trenches in silicon carbide and to planarize our polysilicon trench fill material.

Summary of Research:

Our first objective was to etch deep trenches in silicon carbide. In order to achieve this, a patterned metal mask was used since photoresist and oxide have poor etch selectivity relative to SiC in fluorine-based reactive ion etches (RIE).

A metal layer was first deposited on to the bare SiC surface. Photoresist was then applied and lithographically patterned on the metal layer. The trench pattern was then etched into the metal using a chlorine ICP etcher, the PT770, exposing the SiC. Finally, the Oxford Cobra ICP was then used to etch the deep trenches into the exposed SiC using SF_6-based chemistry. The depth of the trench features were measured using the P10 profilometer.

Thick undoped polysilicon was then deposited to fill the deep trenches. In order to remove the polysilicon from non-trench areas and also to planarize the polysilicon over the trenches, chemical-mechanical polishing (CMP) was used.

Additional work still needs to be completed in order to determine whether this process was satisfactory, such as using a scanning electron microscope (SEM) to determine whether the trenches have been completely filled. In addition to this, metal line test features need to be deposited over the array of deep trenches and electrically tested to confirm that they are shorted across the array, verifying that they are not breaking over the trenches.

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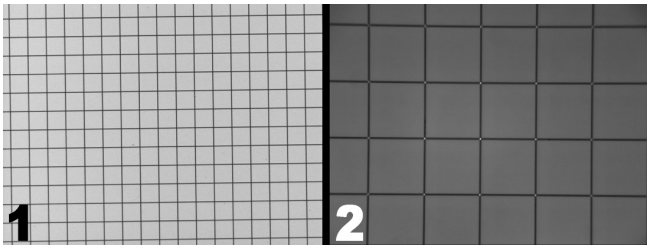

Figure 1, left: Trench features etched into the metal mask. Figure 2, right: Trench features etched into the SiC wafer, no metal mask present.

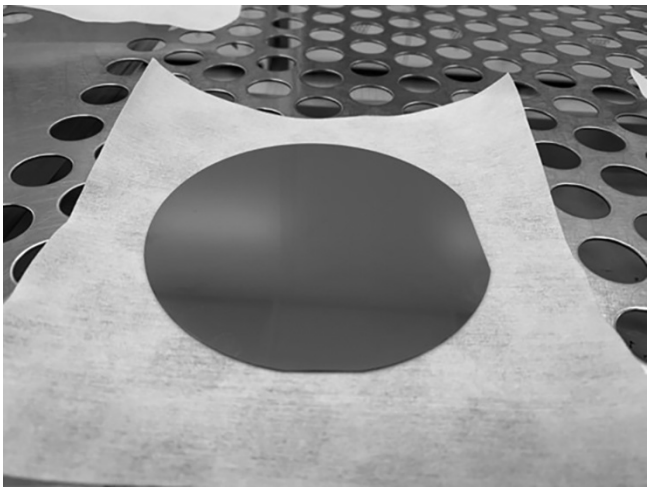

Figure 3: Thick polysilicon on SiC.

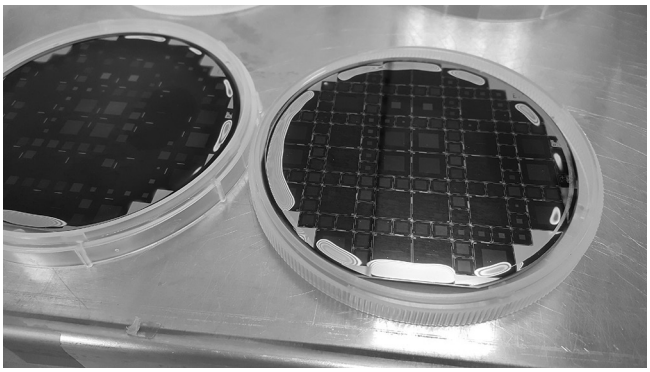

Figure 4: Post-polysilicon CMP.

Emerging III-Nitride Devices for Terahertz Electronics

CNF Project Number: 2800-19

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Primary CNF Tools Used: Veeco AFM, ABM contact aligner, YES Asher, odd-hour evaporator, PT770 etcher, P10 and P7 profilometer, Oxford ALD, Oxford 81 etcher, AJA sputtering

Abstract:

In the present work, we report the design, fabrication and demonstration of emerging III-nitride electronic devices that hold the promise for the manufacture of high-power ultra-fast electronic amplifiers and complementary logic based solely on nitride semiconductors. A novel design of a quantum well transistor is presented and its power performance is assessed employing the Johnson figure-of-merit. The complementary III-nitride p-channel transistor is also studied here, showing record performance in terms of on-current and carrier density. Finally, vertical resonant tunneling transport is also studied in III-nitride heterostructures. By introducing an analytical quantum transport model for III-nitride resonant tunneling diodes (RTDs), we reproduce all the features of the experimentally measured tunneling current. These advances pave the way for the design all-nitride high-power ultra-fast amplifiers and digital integrated circuits.

Summary of Research:

III-nitride materials have emerged as a promising platform for the development of electronic devices capable of meeting the increasing demand for high-power ultra-fast amplifiers for communication networks, and complementary transistors for computing applications. This revolutionary family of wide bandgap semiconductors has already enabled the manufacture of high-power electronic switches, harnessing the internal polarization fields for the generation of highly dense two-dimensional electron gases (2DEG) [1]. However, digital applications require the manufacture of the complementary 2D hole gas (2DHG) switch, which would unleash the full potential of III-nitride semiconductors for digital applications.

In this report, we present important advances in the design, fabrication and understanding III-nitride switches that can be employed for the development of the nitride-based complementary logic for computation, and ultra-fast resonant tunneling diodes (RTDs) that hold the promise for the development of future nitride-based terahertz electronics.

Polarization-induced high-electron mobility transistors (HEMTs) are the workhorse of nitride electronics. HEMTs harness the high electron density of the 2DEG induced at the AlGaN/GaN heterointerfaces.

In the present work, we report a novel design in which a 2DEG is engineered employing AlN as the buffer layer, thus taking advantage of the higher thermal conductivity of the AlN platform. The 2DEG confinement is provided by a 30-nm GaN quantum well sandwiched between the AlN buffer region and a 2-nm AlN top barrier as shown in Figure 1(a). Transistors are fabricated employing a realigned last-gate process with non-alloyed ohmic contacts [2]. Figure 1(b) shows the output characteristics measured at room temperature, revealing a saturation current of 2A/mm and a low on-resistance of 1.3 Ωmm. The transfer curve for this quantum-well HEMT design is displayed in Figure 1(c), showing a current modulation that spans four orders of magnitude with a peak transconductance of 0.6 S/mm. To assess the high-power performance of these devices, breakdown voltage is measured in multiple devices, resulting in a maximum breakdown voltage of 591 Volts.

In addition to III-nitride quantum well HEMTs, the complementary p-type transistor, enabled solely by polarization engineering, is also introduced here. The heterostructure is grown by molecular beam epitaxy (MBE) atop an AlN-template substrate [3]. The MBE-grown layers comprise an AlN buffer layer, an unintentionally (UID)-doped GaN layer extending 5 nm and a 10 nm p-type GaN layer that facilitates the formation of ohmic contacts [See Figure 2(a)]. Enhancement mode p-channel field-effect transistors (pFETs) are fabricated employing a gate-recess process. The transistor characteristics are displayed in Figure

2(b), revealing a record-high on-current of 10 mA/mm and a 640-Ωmm on-resistance. Figures 2(c) shows that the drain current is modulated over four orders of magnitude with a maximum transconductance of 1.5 mS/mm. These results constitute a significant improvement in state-of-art III-nitride pFETs, raising hopes for the demonstration of nitride-based digital ICs.

So far we have discussed the DC operation of III-nitride switches, however high-data rate communication networks also require ultra-fast amplifiers that operate at frequencies approaching the terahertz band. To push the cutoff frequencies of III-nitride high electron mobility transistors (HEMTs) towards this frequency band, parasitic management techniques and highly-scaled fabrication processes have been recently employed [4,5]. However, amplification at frequencies > 1 THz is yet to be demonstrated; in this scenario, alternative gain mechanisms such as resonant tunneling injection, have been proposed to achieve terahertz power amplification [6]. The recent successful engineering of resonant tunneling injection in III-nitride heterostructures [7] has led to an invigorated effort to harness the multiple advantages of nitride-based resonant tunneling devices. Because of their noncentrosymmetric crystal structure, sheets of polarization charge are induced at the heterointerfaces of nitride heterostructures, which lead to a redistribution of free carriers across the active region and surrounding contacts. To get a further insight into the effects of the internal polarization fields, we have recently introduced a quantum transport model that captures the physics of resonant tunneling transport across polar heterostructures.

To experimentally study resonant tunneling transport, we fabricate a series of resonant tunneling diodes (RTDs) with the device structures shown in Figure 3(a). Reflection high-energy electron diffraction (RHEED) is employed to monitor the incorporation of single atomic monolayers to the AlN tunneling barriers [8]. Devices are fabricated employing a self-aligned process and the current-voltage characteristics are measured at room temperature as shown in Figure 3(b). Clear and repeatable negative differential conductance is measured in each of the fabricated samples. Figure 3(b) shown the exponential relationship between the barrier thickness and the resonant tunneling current. Finally, we develop a comprehensive quantum transport model that completely captures all the experimentally measured features of the tunneling current. This model provides a clear insight into the polar RTD current-voltage characteristics and its connection with the heterostructure design parameters. This theory can be employed for the design of nitride resonant tunneling devices exhibiting efficient current injection and improved tunneling dynamics as required in practical applications.

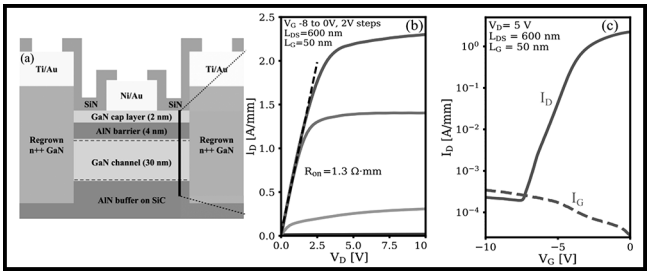

Figure 1: (a) Schematic cross section of the quantum well high-electron mobility transistor (HEMT). (b) and (c) Output and transfer characteristics of the device fabricated at CNF.

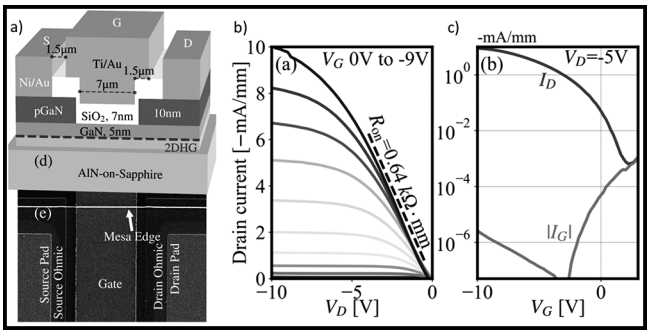

Figure 2: (a) Schematic cross section of the III-nitride p-type field effect transistor (pFET) fabricated in CNF. (b) Room-temperature current-voltage output characteristics show a record-high saturation current of 10 mA/mm and low on-resistance. (c) Transfer characteristics showing four orders of drain current modulation and a peak transconductance of 1.6 mS/mm.

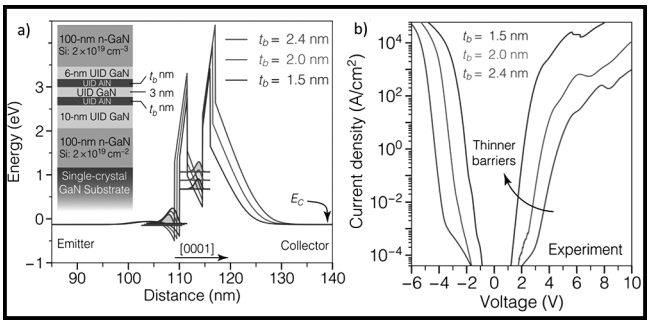

Figure 3: (a) Schematic cross section and band diagram of three resonant tunneling diodes grown by molecular beam epitaxy on single-crystal GaN substrates. (b) Room-temperature current-voltage characteristics for each of the fabricated diodes showing the exponential modulation of the tunneling current as a function of barrier thickness.

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Fully Passivated InAlN/GaN HEMTs on Silicon with f_T/f_{MAX} of 144/141 GHz

CNF Project Number: 2800-19

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Primary CNF Tools Used: Autostep i-line stepper, Heidelberg mask writer DWL2000, P7 profilometer, FilMetrics, AFM Veeco Icon, Zeiss SEM, PT770, Oxford81, Oxford PECVD, Oxford ALD, odd-hour evaporator, AJA sputter deposition, RTA AG610, JEOL9500

Abstract:

Depletion-mode high-electron mobility transistors (HEMTs) based on a quaternary barrier $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructure on a Si substrate were fabricated. The 87 nm long gate device shows a dc drain current density of 2.48 A/mm, a peak extrinsic transconductance of 450 mS/mm, and balanced current gain cutoff frequency f_T and maximum oscillation frequency f_{MAX} are 144 and 141 GHz, respectively.

Summary of Research:

Gallium nitride (GaN)-based high electron mobility transistors (HEMTs) have demonstrated great potential for high-speed, high power RF applications [1] and next-generation power electronics [2]. In addition, the adoption of a Si substrate would pave the way for low cost and high-performance GaN electronics.

We report the fabrication and DC and RF characteristics of fully passivated InAlN/GaN high-electron mobility transistors (HEMTs) on Si substrates with balanced f_T and f_{MAX} (144/141 GHz).

The InAlN/AlN/GaN HEMT structure consists of a 10 nm $In_{0.17}Al_{0.83}N$ barrier, a 1 nm AlN spacer (total barrier thickness: 11 nm), a 800 nm unintentionally doped GaN channel, and AlGaN/AlN buffer and nucleation layers on a 6" Si substrate, grown by a Propel® HVM MOCVD system at Veeco Instruments. Room temperature Hall-effect measurements prior to device fabrication showed a 2DEG sheet concentration of $2.4 \times 10^{13}/cm^2$ and electron mobility of 1310 $cm^2/V{\cdot}s$, corresponding to a sheet resistance of 196 Ω/sq.

A schematic cross-section of the InAlN/AlN/GaN HEMT device with regrown n^+ GaN contacts is shown in Figure 1(a). The device fabrication process started with patterning of a SiO_2 mask for n^+GaN ohmic regrowth by PA-MBE. The preregrowth etch depth into the HEMT

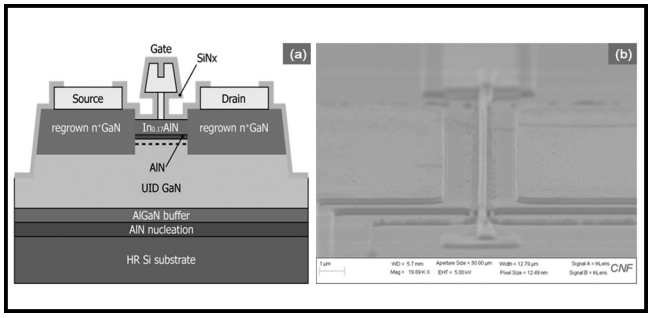

Figure 1: (a) Schematic cross-section of fully passivated InAlN/AlN/GaN HEMTs on Si with regrown n+GaN contacts. (b) An angled SEM image of a fabricated InAlN/AlN/GaN HEMT with an EBL T-gate.

structure was 40 nm, and regrown n^+GaN was 100 nm with a Si doping level of $7 \times 10^{19}/cm^3$. Non-alloyed ohmic contact of Ti/Au/Ni was deposited by e-beam evaporation. T-shaped Ni/Au (40/200 nm) gates were formed by electron-beam lithography, followed by liftoff. The devices were finally passivated by a 50 nm PECVD SiN_x. TLM measurements yielded a contact resistance of 0.19 Ω·mm. The device presented here has a regrown n^+GaN source-drain distance L_{sd} of 800 nm, a gate width of 2 × 25 μm, and a gate length L_g of 87 nm. Figure 1(b) shows an angled-SEM image of the fabricated InAlN/AlN/GaN HEMT.

Figure 2(a) shows the family *I-V* curves of the device, measured for V_{ds} = 0 to 8 V and V_{gs} = 1 to -8 V. The device has a saturation drain current I_{dss} = 2.48 A/mm and an on-resistance R_{on} = 1.07 Ω·mm extracted at V_{gs} = 1 V. The transfer curves are shown in Figure 2(b). A peak extrinsic transconductance g_m is ~ 0.45 S/mm at V_{ds} = 5 V. Figure 3(a) shows the current gain $|h_{21}|^2$ and unilateral gain *U* of the device as a function of frequency at the peak f_T bias condition, V_{ds} = 5 V, and V_{gs} = -4.6 V. The extrapolation of both $|h_{21}|^2$ and *U* with -20 dB/dec slope gives the current gain cutoff frequency/maximum oscillation frequency f_T / f_{MAX} of 144/141 GHz after de-embedding. The f_T and f_{MAX} of the device are summarized in Figure 3(b). Figure 3(b) shows how the results of this device compare with the early state-of-art results of GaN HEMTs on Si substrates [3,4].

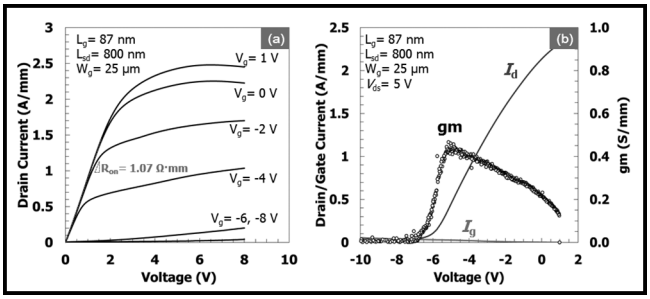

Figure 2: (a) Family I-V curves and (b) transfer characteristics of the device with L_g *= 87 nm and* L_{sg} *= 800 nm.*

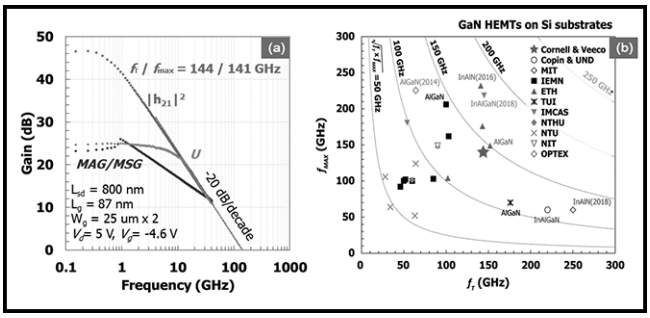

Figure 3: (a) Current gain and unilateral gain of the device with L_g *= 87 nm, showing* f_T / f_{MAX} *= 144/141 GHz. (b) Comparison of the measured* f_T *and* f_{MAX} *of GaN HEMTs on Si substrates.*

References:

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