# Electrical Characterization of $In_2Ga_2ZnO_7$ Crystallized by Millisecond Heating

**CNF Project Number: 150-82**

**Principal Investigator: Michael O. Thompson**

**User: Katherine K. Quinn**

*Affiliation: Materials Science and Engineering, Cornell University*

*Primary Source of Research Funding: Air Force Office of Scientific Research (AFOSR)*

*Contact: mot1@cornell.edu, kkq2@cornell.edu*

*Website: http://thompson.mse.cornell.edu/*

*Primary CNF Tools Used: Furnace B2, Oxford 100 PECVD, Plasma-Therm 720, CHA evaporator, SÜSS MicroTech MA6*

**Abstract:**

**In this work, we examined the electrical properties of $In_2Ga_2ZnO_7$ films crystallized by laser spike annealing (LSA) for a dwell time of 10 ms. Using the lateral gradient LSA method, samples were annealed and crystallization was visibly observed. Spatially resolved sheet resistance measurements were attempted across the LSA stripe using patterned van der Pauw structures. Films as annealed were insulating with a conductance below $10^{-8}$ S and exhibited only capacitor-like behavior. Analysis suggests that a thin $SiO_2$ passivation layer remained on films during processing leading to the observed behavior.**

## Summary of Research:

Over the past two decades, various amorphous oxide semiconductors have been explored as alternatives to amorphous hydrogenated silicon used in thin film transistors for large area displays. The $In_2O_3$-$Ga_2O_3$-ZnO (IGZO) material system in particular exhibits promising electrical characteristics including high electron mobility and stable carrier concentration. However, devices fabricated with amorphous IGZO (α-IGZO) are limited by turn-on voltage instabilities. While crystalline forms of IGZO maintain favorable electrical characteristics and do not exhibit device instabilities like α-IGZO, only films formed during heated substrate depositions have been studied. Alternatively, it is possible to crystallize α-IGZO films on short time scales (250 μs to 10 ms) using laser spike annealing techniques, however, very little is known about the electronic properties of metastable crystallized alloys in the IGZO system.

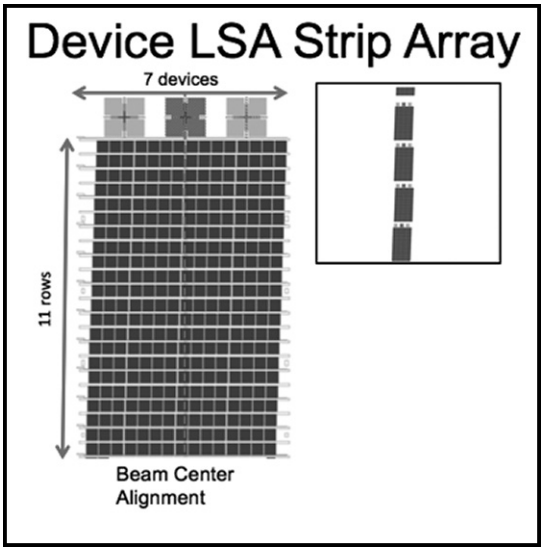


*Figure 1: Schematic of van der Pauw device subarray consisting of 11 rows containing seven devices each. Above each subarray are alignment marks used to align the beam center during LSA. Inset is approximate scale of one device stripe on a 2 cm × 2 cm sample.*

Van der Pauw devices were fabricated on lightly doped *p*-type Si wafers with ~ 80 nm of thermally grown $SiO_2$ for the purposes of electrical characterization (Furnace $B_2$). Amorphous thin film samples of $In_2Ga_2ZnO_7$ were deposited onto rotating substrates using a reactive RF magnetron sputtering system in a 10% $O_2$ in Ar mix with 120 W power. An ~ 30 nm thick passivating layer of $SiO_2$ was deposited to protect the IGZO surface (Oxford 100 plasma-enhanced vapor deposition). Samples were photolithographically patterned to form van der Pauw structure arrays, as shown in Figure 1 (SÜSS MicroTech MA6). The $SiO_2$ passivation layer was patterned using fluorine-based dry etching (Plasma-Therm 720) and IGZO was patterned using 2 wt.% HCl wet etching. After patterning, samples were annealed at 350°C with 7 sccm $N_2$ for 30 min in a quartz tube furnace.

Lateral gradient LSA (lgLSA) was used to crystallize the films. LSA uses a line-focused continuous wave laser beam to scan across a sample for controlled time durations (dwell). In lgLSA, the beam is intentionally non-uniform orthogonal to the scanning direction to produce a lateral temperature profile across the device row, allowing for electrical characterization as a function of peak annealing temperature.

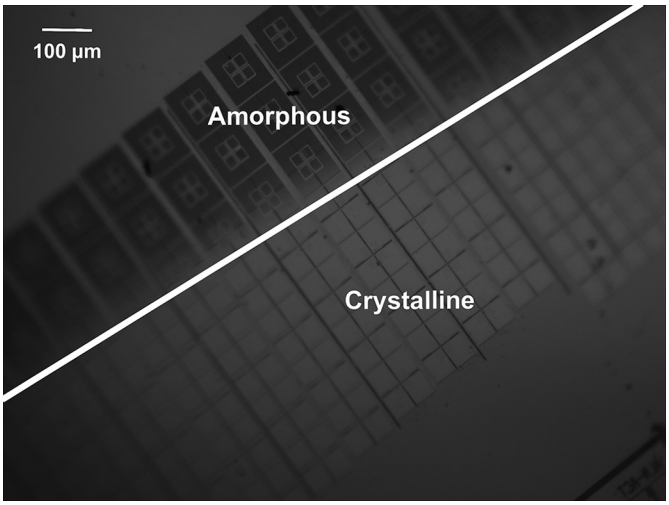


*Figure 2: Evident structural transition indicated by color change along row of devices resulting from anneal by diode laser at 70.9 A for 10 ms dwell.*

Samples were irradiated with fiber-coupled diode laser (980 nm wavelength, 1.5 mm full width half maximum) for 10 ms dwells, achieving expected anneal peak temperatures above and below a known Si melt temperature of 1414°C. Figure 2 shows a photomicrograph of an anneal stripe that produced a dark to light color gradient across the device rows, confirming a structural transition from an amorphous structure to the crystalline phase within the lateral temperature gradient.

Metal contacts were deposited (CHA Evaporator) and patterned using liftoff. Electrical measurements of devices were conducted using a 4-point manual probe station and a Keithley 2400 Source Measurement Unit (SMU) to supply current and measure voltage. Contact resistance and 4-point van der Pauw resistance measurements were obtained.

Initial resistance measurements ranged in the 60-200 MΩ range, indicating essentially non-conducting films. In contrast to the expected linear behavior of a conductive material, the IV characteristics showed parabolic curvature as seen in the resistance scans in Figure 3. This behavior is consistent with the material acting as a capacitor in that the material charges to a voltage at the application of negative current, then begins discharging symmetrically when the direction of current is reversed. The capacitance of the van der Pauw devices was extracted and found to be 96 pF.

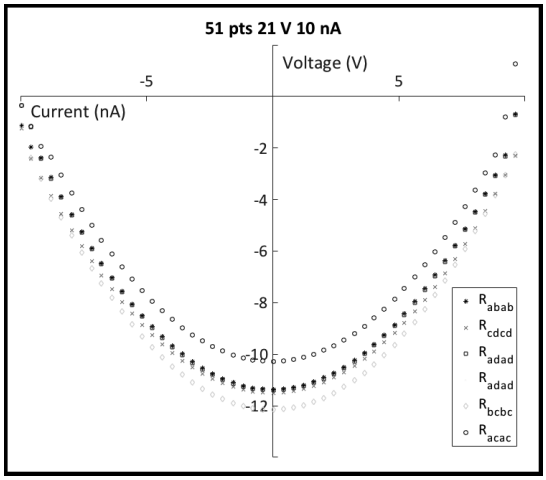


*Figure 3: 4-point van der Pauw resistance measurements at 10 nA exhibited a parabolic IV curve, indicating the charging and discharging of current that is characteristic to capacitor behavior.*

This implied that a material in the device stack was non-conducting and contributing to the measured device capacitance. The $SiO_2$ passivation layer, the active IGZO layer, and the thermally-grown $SiO_2$ layer on the Si substrate were considered as possible sources of the capacitance. After comparing the estimated layer thickness of each material to a calculated thickness required to yield a 96 pF capacitance, it was found that only a thin remainder of the passivation $SiO_2$ layer could be responsible for the capacitance. The most probable explanation for this observed capacitance is that the $SiO_2$ passivation layer was not completely etched during processing of the van der Pauw devices, resulting in a dielectric layer between the IGZO and the metal contacts. This motivates future improvements in the etching techniques used in the fabrication of devices.

## References:


[1] Kamiya, Toshio and Hosono, Hideo. (2010). "Material characteristics and applications of transparent amorphous oxide semiconductors." NPG Asia Materials. 2, pp. 15-22. DOI: 10.1038/asiamat.2010.5.

[2] Lynch, David. (2017). "Indium Gallium Zinc Oxide: phase formation and crystallization kinetics during millisecond laser spike annealing." (Doctoral dissertation).

[3] Yamazaki, Shunpei. (2013). "A possibility of crystalline Indium-Gallium-Zinc-Oxide," Fifth Asia Symposium on Quality Electronic Design (ASQED 2013), pp. 1-5. DOI: 10.1109/ASQED.2013.6643553.

[4] Chung, Chen-Yang. (2016). "High mobility of sputtered $In_2Ga_2ZnO_7$ (IGZO) thin film transistors (TFTs)." (Doctoral dissertation).

[5] Bell, Robert. (2016). "Lateral Temperature-Gradient Method for High-Throughput Characterization of Material Processing by Millisecond Laser Annealing." ACS Combinatorial Science. 18, pp. 548.558. DOI: 10.1021/acscombsci.6b00043.