$MoS_2/PtSe_2$ MOSFETs and CMOS Integration

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Primary CNF Tools Used: ABM contact aligner, Autostep i-line stepper, PT720-740 etcher, SC4500 odd-hour evaporator, P10 profilometer

Abstract:

We have used an alternative approach to the current practice of mechanical exfoliation and e-beam lithography in fabricating transitional metal dichalcogenide metal oxide semiconductor field effect transistors (TMD MOSFETs). The alternative uses a CMOS back-end-of-line (BEOL) process and large-scale transfer/dispense or direct thermal conversion. The BEOL process allows buried gates as short as 0.1 μm and high-quality gate insulator to be fabricated before TMD deposition [Figure 1(a)]. Large-scale transfer/dispense or thermal conversion provides large area of TMDs at low temperature tolerable by the BEOL process. After further photolithography, approximately 1,500 RF-probeable MoS_2 or $PtSe_2$ MOSFETs were fabricated on each chip [Figure 1(c)]. The resulted MOSFETs were then characterized, which showed state-of-art performances with high yields. This work demonstrates that it is practical and promising to integrate TMDs or other 2D devices with CMOS circuits.

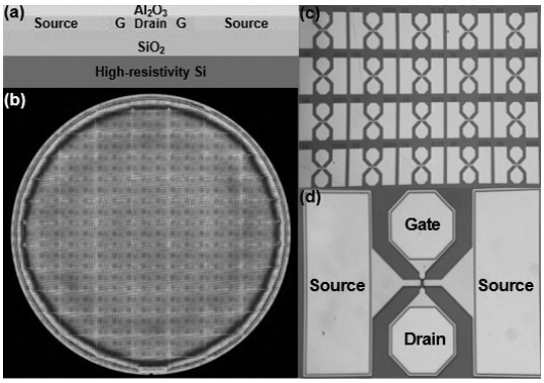

Figure 1: (a) Cross-sectional schematic of buried gates and micrographs of (b) a 200-mm Si wafer with approximately sixty 25 mm × 15 mm chips, (c) part of a 25 mm × 15 mm chip with rows and columns of MOSFETs totaling approximately 1,500 on each chip, and (d) details of each RF-probable MOSFET with gate width of approximately 10 μm and gate length of approximately 0.2, 0.4 or 0.6 μm.

Summary of Research:

For chemical vapor deposited and transferred molybdenum diselenide (MoS_2) films, the fabricated MoS_2 MOSFETs showed yield greater than 50% in terms of effective gate control with less-than-10 V threshold voltage, even for MOSFETs having deep-submicron gate length [1]. The large number of fabricated MOSFETs allowed statistics [Figure 2(c) and (d)] to be gathered and the main yield limiter to be attributed to the weak adhesion between the transferred MoS_2 and the substrate. With cut-off frequencies approaching the gigahertz range [Figure 2(b)], the performances of the MOSFETs were comparable to that of state-of-the-art MoS_2 MOSFETs, whether the MoS_2 was grown by a thin-film process or exfoliated from a bulk crystal.

For solution-processed and dispensed MoS_2 films, nearly 100% yield was achieved and the cut-off frequencies were measured for the first time to be on the order of 100 MHz [2]. Being low temperature, low cost, and large area, solution-processed MoS_2 is attractive for future-generation thin-film and flexible transistors. To obtain the optimum combination of effective gate control and low contract resistance, channel recess was demonstrated for the first time on MoS_2. Specifically, channel recess by CHF_3/O_2 dry etching up to 60s was performed on submicron buried-gate MOSFETs fabricated on 20-nm-thick spin-coated MoS_2. It was found that the channel recess improved the current on/off ratio by three orders of magnitude while maintaining approximately the

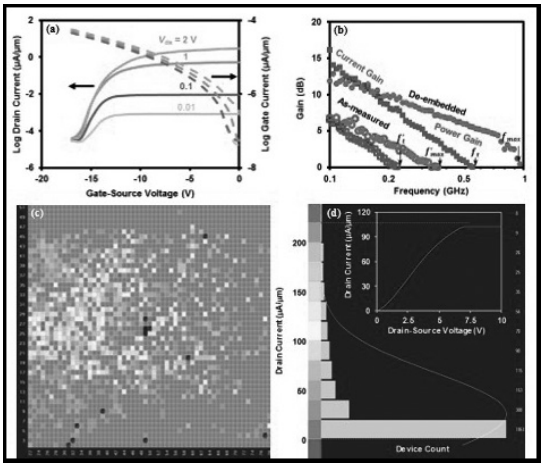

Figure 2: (a) Measured transfer characteristics of a typical MoS_2 MOSFET, (b) forward current-gain cut-off frequency f_T and maximum frequency of oscillation f_{MAX} of a typical MoS_2 MOSFET after annealing at 300°C for 1h in vacuum. V_{GS} = 0.2 V; V_{DS} = 3 V, (c) wafer map, and (d) histogram of maximum drain-source current measured with gate floating and V_{DS} = 10 V across a 15 mm × 15 mm area. The curve in (d) indicates Gaussian fitting with a peak around 30 μA/μm. Inset in (d) illustrates drain current saturation behavior.

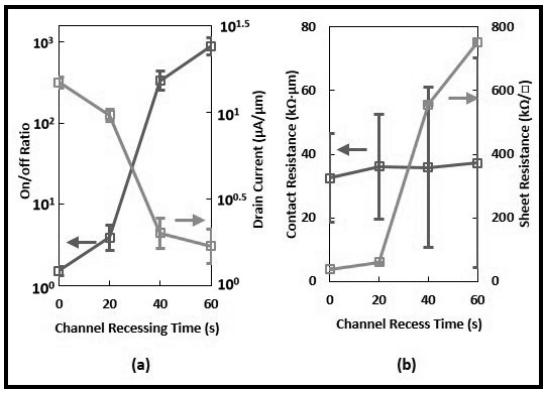

Figure 3: Evolution of (a) on/off ratio (V_{DS} = 1V) and drain current (V_{DS} = 1V, V_{GS} = 0), (b) contact and sheet resistances extracted from TLM test structures of 20 nm MoS_2.

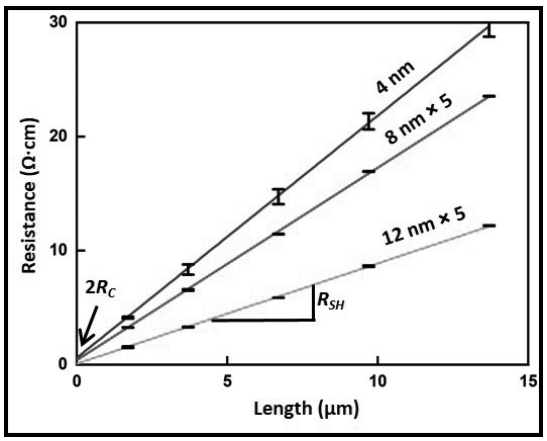

Figure 4: Total resistance RT measured on TLM structures of different channel lengths and $PtSe_2$ thicknesses.

same contact resistance and peak transconductance as that of a uniformly 20-nm-thick channel (Figure 3). The resulted performance was among the best of all solution-processed MoS_2 MOSFETs [3]. The same channel recess technique can be used to improve the performance of MOSFETs made of other 2D materials.

Wafer-scale fabrication of platinum diselenide ($PtSe_2$) MOSFETs was demonstrated for the first time by photolithography on Pt films directly selenized at 400°C. Taking advantage of the unique property of $PtSe_2$ to transition from semiconductor to semimetal as its thickness increases beyond a few monolayers, channel recess was adapted for improving gate control while keeping the contact resistance as low as 0.008 Ω·cm (Figure 4). The wafer-scale fabrication resulted in uniform device characteristics so that average vs. best results were reported, as well as RF vs. DC characteristics.

For example, the drain current at V_{GS} = -10, V_{DS} = -1 V were 25 ± 5, 57 ± 8, and 618 ± 17 μA/μm for 4-, 8-, and 12-nm-thick $PtSe_2$, respectively [4]. The corresponding peak transconductances were 0.20 ± 0.1, 0.60 ± 0.05, and 1.4 ± 0.1 μS/μm. The forward-current cut-off frequency of 12-nm-thick $PtSe_2$ MOSFETs was 42 ± 5 MHz, whereas the corresponding frequency of maximum oscillation was 180 ± 30 MHz. These results confirmed the application potential of $PtSe_2$ for future generation thin-film transistors.

All MoS_2 and $PtSe_2$ tested to date show compatibility with complementary metal oxide semiconductor (CMOS) process and state-of-art RF performances. To reduce the contact resistance while maintaining gate control, a channel-recess process was developed which showed promising results. Channel recess will be further optimized in the future.

References:

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