Device Processes and Electrical Characteristics of First 1 kV Ga_2O_3 Vertical Power Transistors

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Abstract:

High-voltage vertical Ga_2O_3 MISFETs are developed employing halide vapor phase epitaxial (HVPE) layers on bulk Ga_2O_3 <001> substrates. The low charge concentration of ~ 10^{16} cm^{-3} in the *n*-drift region allows three terminal breakdown voltages to reach up to 1057 V without field plates. The devices operate in the enhancement mode with a threshold voltage of ~ 1.2-2.2 V, a current on/off ratio of ~ 10^8, and an on-resistance of ~ 13-18 mOhm·cm^2, and an output current of > 300 A/cm^2. This is the first report of high-voltage vertical Ga_2O_3 transistors with enhancement mode operation, a significant milestone toward realizing Ga_2O_3-based power electronics.

Summary of Research:

Gallium oxide (Ga_2O_3) has emerged as a new semiconductor material for high-power applications in recent years. As the most stable form monoclinic β-Ga_2O_3 has been reported with a wide bandgap up to 4.9 eV, a high expected breakdown electric field up to 8 MV/cm and a decent intrinsic electron mobility limit of 250 cm^2/Vs, which enables high-voltage and high-power operation. The experimentally reported critical electric field up to 5.2 MV/cm already exceeds that of SiC and GaN, and electron mobility of 100-150 cm^2/Vs has been achieved in both bulk substrates as well as epitaxial layers. In addition, low-cost, large area single-crystal substrates allow high-quality epitaxial layers to be developed using various methods.

The past few years witnessed successful development of Ga_2O_3 lateral FETs including MOSFETs, MESFETs, nano-membrane FETs and FinFETs and vertical diodes such as SBDsand hetero-junction *p-n* diodes. However, high performance vertical power transistors on Ga_2O_3 have only been demonstrated by our group [1,2].

There are several reasons: (1) vertical power transistors require high quality epitaxial layers with minimized impurity incorporation and precisely controlled doping concentrations, (2) Vertical transistor structure design and fabrication processes are more complicated than those of lateral transistors and diodes.

In this report, we summarize the most recent development and results of Ga_2O_3 vertical transistors in our group.

We are able to combine high quality epitaxial Ga_2O_3 layers with a fully vertical Ga_2O_3 transistor process flow, and demonstrate the first 1-kV class vertical Ga_2O_3 MISFETs (or FinFETs). In addition to the high breakdown voltage, the transistor also shows

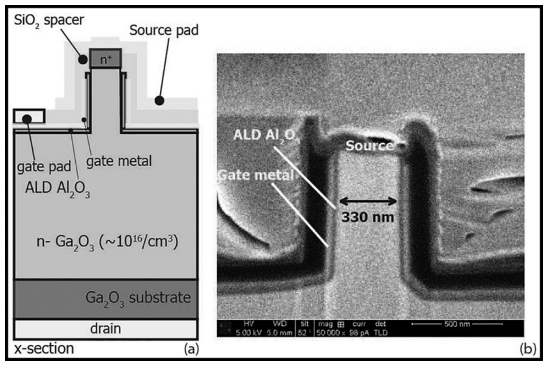

Figure 1: (a) Schematic cross-section of a Ga_2O_3 vertical power MISFET. (b) 52° SEM cross-section image of a completed Ga_2O_3 vertical Fin-MISFET showing a 330 nm wide and 795 nm long channel.

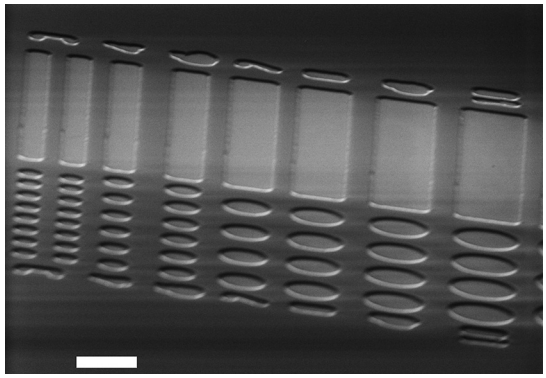

Figure 2: Representative I_d-V_{ds} characteristics of a Ga_2O_3 vertical power MISFET.

enhancement-mode operation, which is a desired feature for application as power switches.

The epitaxial layers were grown by HVPE on *n*-type bulk Ga_2O_3 <001> substrates (n = 2 × 10^{18} cm^{-3}). The 10-mm thick *n*-Ga_2O_3 epitaxial layer is doped with Si with a target doping concentration of < 2 × 10^{16} cm^{-3}.

The schematic device structure is depicted in Figure 1. A simplified process flow is described as the following:

1. Si Implantation for Top Ohmic Contacts

- SiO_2 mask deposition (Oxford PECVD)
- Si implantation with a box profile of 1E20 cm^{-3}
- Activation annealing at 1000°C in furnace

2. Vertical Channel Definition

- E-beam lithography and Pt metal mask deposition
- Low power ICP-RIE dry etching of Ga_2O_3
- Target channel width/height ratio of 0.3/1.0 μm

3. Gate Metallization

- Deposition of ALD Al_2O_3 ~ 30 nm
- Sputtering Cr ~ 50 nm to cover the sidewalls of the channel
- E-beam evaporation of Ti/Au as gate metal pads

4. Gate-Source Spacer Formation

- Photoresist planarization and thinning to expose top of Ga_2O_3 channels.
- Etch back ALD Al_2O_3 and Cr by dry etching
- PECVD SiO_2 spacer deposition ~ 200 nm
- Photoresist planarization and thinning
- SiO_2 spacer etch back

5. Source and Drain Metallization

- Sputter Ti/Al/Pt source metals
- Sputter Ti/Al/Pt back drain contacts

The net charge concentration (N_D-N_A) in the *n*-Ga_2O_3 drift layer is estimated at 1 × 10^{15} - 1.2 × 10^{16} cm^{-3} using capacitance-voltage (C-V) measurements. The low charge concentration is essential to realize E-mode operation and high breakdown voltages.

Figure 2 shows the representative I_d-V_{ds} family curves of a fabricated vertical Ga_2O_3 MOSFET with a source area of 0.33 mm × 80 mm.

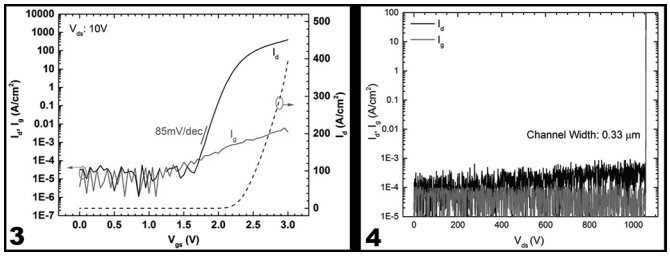

Figure 3, left: *Representative* I_d/I_g-V_{gs} *transfer characteristics in the semi-log and linear scale, along with the extracted subthreshold slope.* ***Figure 4, right:*** *Representative three-terminal off-state (at* V_{gs} *= 0 V)* I_d/I_g-V_{ds} *characteristics and breakdown voltage of* Ga_2O_3 *vertical power MISFETs.*

At V_{gs} of 3 V and V_{ds} of 10 V, the drain current reaches ~ 350 A/cm^2 with an associated differential on-resistance of ~ 18 mW·cm^2, normalized to the area of the $n^+Ga_2O_3$ source. The representative I_d-V_{gs} transfer characteristics of these devices are shown in Figure 3.

The V_{th} defined by linear extrapolation of the drain current at the peak transconductance is ~ 2.2 V. The sub-threshold slope is measured to be ~ 85 mV/dec near a current density of 1 mA/cm^2 and the hysteresis is less than 0.2 V. The off-state leakage currents and 3-terminal breakdown voltages in these vertical power MISFETs are measured at V_{gs} = 0 V.

The representative results are plotted in Figure 4: both the drain and gate leakage currents remain low, near the detection limit of the measurement instrument, before the hard breakdown near 1057 V. Two-dimensional device simulations reveal that the electric field peaks near the outer edges of the gate pads. In fact, examination of the devices after breakdown shows visible damage near the outer edges of the gate pads. Therefore, we expect that higher breakdown voltages be achieved by implementing field plates or ion implantation edge termination techniques.

References:

[1] Z. Hu, K. Nomoto, W. Li, L. J. Zhang, J.-H. Shin, N. Tanen, T. Nakamura, D. Jena and H. G. Xing, "Vertical fin Ga_2O_3 power field effect transistors with on/off ratio > 10^9", Device Research Conf. (DRC), pp. 1-3. DOI: 10.1109/DRC.2017.7999512, June 2017.

[2] Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena and H. G. Xing, "Enhancement-mode Ga_2O_3 vertical Transistors with breakdown voltage > 1 kV", IEEE Electron Device Lett., Vol. 39, No. 6, pp. 869-872. DOI: 10.1109/LED.2018.2830184, June, 2018.