

Development of Scanning Graphene Hall Probes for Magnetic Microscopy

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Primary CNF Tools Used: Veeco Icon AFM, Zeiss Supra SEM/Nabity, odd-hour evaporator, even-hour evaporator, Trion etcher, 5x stepper, Oxford 100 etcher, Plasma-Therm Versaline

Abstract:

We discuss our progress on developing scanning Hall probes using graphene as the sensitive material, with the goal to perform magnetic imaging experiments with submicron resolution. Our devices demonstrate a promising Hall sensitivity at cryogenic temperatures competitive with that of commercially available Hall probes. We plan to include a deep etch surrounding the sensitive area of the device to facilitate alignment and scanning over samples.

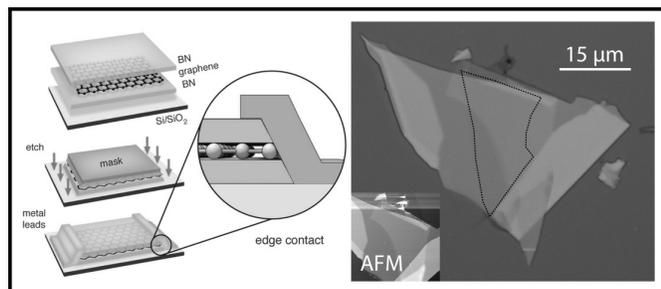


Figure 1: Left panel: overview of process from [3], used with permission. Right panel: a monolayer graphene flake (dotted outline) sandwiched between flakes of hexagonal boron nitride. Inset: AFM image, scaled down.

Summary of Research:

Scanning magnetic probe microscopy is a useful technique to study magnetism and electronic transport in materials because it provides a direct spatial map of the magnetic landscape above the sample surface. We currently use superconducting quantum interference device (SQUID) magnetometers for our imaging experiments, but these probes only operate at low temperatures and magnetic fields under ~ 1 Tesla [1]. In contrast, scanning Hall probes permit imaging in a strong magnetic field, over a much larger temperature range, and with potentially higher spatial resolution than SQUIDs [2]. To compete with the field sensitivity of a SQUID and to enable local fabrication, we choose to fabricate Hall probes from

graphene encapsulated in hexagonal boron nitride (hBN) with one-dimensional edge contacts (Figure 1). Devices made with this architecture possess a remarkably low level of disorder, permitting tunability to low carrier density ($\sim 10^{10} \text{ cm}^{-2}$) to maximize the Hall response while maintaining a high mobility that enables low-noise measurements [3].

Our process is derived from the steps described in Ref. [3], with the important modification to include an aligned top gate in the design (Figure 2, inset), which shields the graphene layer from electrostatic inhomogeneity on the sample. We exfoliate graphene and hBN onto silicon chips and select monolayer flakes of graphene and uniform flakes of hBN using optical and atomic-force microscopy (Veeco AFM). Using the van der Waals assembly technique [3,4], we use a polymer stamp to sequentially pick up and stack a hBN/graphene/hBN heterostructure (Figure 1). We then release the stack onto a heavily doped SiO_2/Si substrate pre-patterned with alignment marks and metal contacts, dissolve the polymer in chloroform for several hours, and anneal in high vacuum at 350°C for three hours.

We again use AFM to identify regions of the stack that are flat and free of bubbles or wrinkles, and then use electron-beam lithography (Nabity) to define a metal (Cr/Au/Pt) top gate in a Hall bar or Hall cross geometry. In a second lithography step, we pattern an etch mask, leaving the edges of the top gate exposed to translate the shape of the topgate directly into the stack. We use an

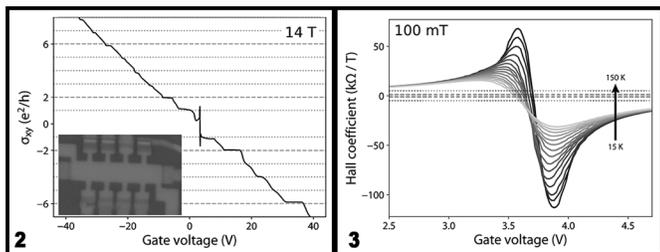


Figure 2, left: Dependence of the Hall conductance on carrier density in a large external magnetic field. The dashed lines indicate expected conductance plateaus for degenerate spin and valley Landau levels, while the dotted lines indicate the conductance plateaus for lifted spin-valley degeneracy. Inset: optical image of the device. **Figure 3, right:** Hall coefficient (sensitivity) of the device from Figure 2 measured at 100 mT and at temperatures from 15 K (dark) to 150 K (light). The light dashed line marks a typical Hall coefficient for GaAs-based Hall probes [8], and the dark dotted line marks the maximum Hall coefficient previously reported for graphene devices at room temperature [7].

inductively coupled plasma of CHF_3 , O_2 , and Ar (Trion etcher) to selectively etch hBN, creating a step-like edge profile exposing a few-nm-wide strip of graphene [5]. In a final electron-beam lithography step, we pattern, deposit, and lift off Cr/Au/Pt contacts overlapping the exposed graphene edge. To protect the devices from mechanical stresses during scanning, we evaporate an ~ 80 nm layer of SiO_2 over the completed device.

We characterize device quality by measuring Hall voltage as a function of back gate voltage in an applied magnetic field. In a large magnetic field (Figure 2), the plateaus of Hall conductance at integer multiples of the conductance quantum demonstrate that the spin-valley degeneracy of the Landau levels is fully lifted, an indication of high device quality [6]. For small magnetic fields, the Hall resistance divided by the magnetic field gives the linear Hall coefficient (Figure 3). On either side of the charge neutrality point (~ 3.7 V), the Hall coefficient reaches a maximum and then falls off inversely with the magnitude of the carrier density. Our first measurements already demonstrate a Hall coefficient competitive with that previously reported for graphene at room temperature and GaAs at cryogenic temperatures [7,8].

To adapt these devices into a geometry suitable for scanning magnetic imaging, we will soon add a deep-

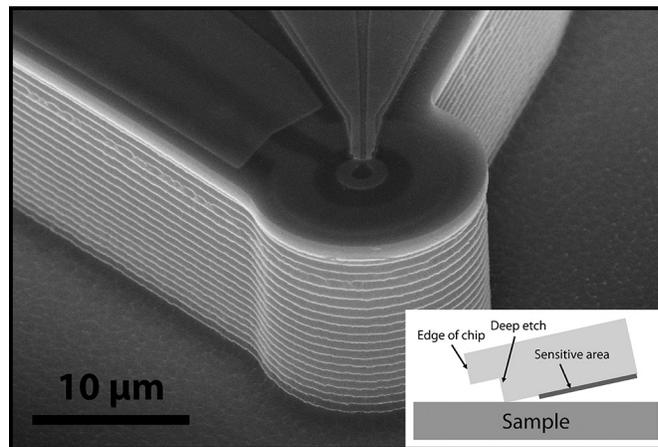


Figure 4: Deep etch surrounding the pickup loop of a SQUID magnetometer.

etched trench surrounding the sensitive area, essentially positioning the Hall cross at the corner of the chip. Figure 4 demonstrates the deep-etch feature added to a SQUID magnetometer, and the inset clarifies the alignment geometry. To achieve this structure, we pattern the chip using photolithography (5x stepper) and etch through the SiO_2 and Si layers (Oxford 100 and Plasma-Therm Versaline) to a total depth of ~ 12 μm . With the inclusion of this final step, the Hall probes will be ready to begin scanning over test samples to characterize the point spread function of the probe and to calibrate the conversion between Hall voltage and magnetic field.

References:

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