Electrical Characterization of Dielectric Films

2023 CNF iREG Intern: Toko Ogata Intern Affiliation: Chemistry, Graduate School of Chemical Sciences and Engineering, Hokkaido University, Hokkaido, Japan

CNF iREG Principal Investigator: Dr. Lynn Rathbun, Cornell NanoScale Facility (CNF), Cornell University CNF iREG Mentors: Jeremy Clark, Phil Infante, Aaron Windsor; CNF, Cornell University

Program & Primary Sources of Research Funding: 2023 Cornell NanoScale Facility International Research Experiences for Graduates (CNF iREG) Program via the NSF under Grant No. NNCI-2025233; NNCI/NIMS Graduate Exchange Fellowship Program administered by Coordination Office, Center of Advanced Research Infrastructure for Materials and Nanotechnology of the National Institute for Materials Science - NIMS Contact: carnation@eis.hokudai.ac.jp, rathbun@cnf.cornell.edu,

clark@cnf.cornell.edu, infante@cnf.cornell.edu, windsor@cnf.cornell.edu

Website(s): https://cnf.cornell.edu/education/reu/2023, https://nanonet.mext.go.jp/page/NNCI-prg.html Primary CNF Tools Used: SC4500 Even-Hour Evaporator, Keithley 4200A - IVCV Testing Station,

Arradiance ALD Gemstar-6, MOS Metal Anneal 3 - C1

Abstract:

The characteristics of dielectric thin films have been studied to improve the performance and sizing of devices, especially semiconductor Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). The MOSFET switches the current flow by inversion on the semiconductor surface as applied voltage across the MOS capacitor. The MOS capacitor is the heart of the MOSFET, because the operation and characterization are dependent on this inversion. Since the performance of the MOS capacitor is strongly affected by the properties of the oxide film, different dielectric materials and deposition tools are expected to have different C-V curves. We compared the C-V curves of devices using different deposition tools and materials, then discussed which is the best to fabricate MOS capacitors.



Figure 1: The schematic of the C-V curve for the n-type MOS capacitor at low frequency voltage (dashed), and high frequency voltage (solid) and three regimes: Accumulation regime (right part), Depletion regime (center part), and Inversion regime (left part).

Summary of Research:

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a three-terminal device, called Gate, Drain, and Source, used for amplifying or switching electronic signals. When the proper voltage is applied to the gate, the semiconductor surface at the interface of oxide and semiconductor is inverted from n-type to p-type or from p-type to n-type, depending on the semiconductor substrate used. The current flows between source and drain. This Metal-Oxide-Semiconductor structure applied the gate voltage known as MOS Capacitor. The MOS capacitor is the heart of MOSFET.

The capacitance of the MOS capacitor changes by sweeping the gate voltage. The Capacitance-Voltage (C-V) characteristic curve provides some useful information. The C-V curves visualize three regimes of the MOS capacitor: Accumulation, Depletion, and Inversion. The voltages at boundaries of regions are called Flat-band Voltage (V_{FB}) and Threshold Voltage (V_{th}), respectively. V_{FB} is defined as the voltage such that there is zero net charge density in oxide material, and V_{th} as the minimum voltage required to create an inversion layer. These are one of the most important parameters that can be extracted from C-V curves. Since the characteristics of the MOS device is strongly affected by the oxide films, the C-V curve also gives properties of oxide films such as the permittivity. Figure 1 shows the schematic of the C-V curve for the n-type MOS capacitor.

Therefore, we measured the C-V curve for device characterization, and compared the differences in deposition tools and materials, to find which is the best to fabricate MOS capacitors. MOS capacitors, consisting of an aluminum electrode, a dielectric film of various materials, and a n-type silicon substrate body, were made by a simple process: 20-50 nm silicon dioxide (SiO_2) , hafnium oxide (HfO_2) , zirconium dioxide (HfO_2) , and aluminum oxide (Al_2O_3) films were formed on the n-type silicon wafer, then 200 nm of aluminum was deposited through a shadow mask. Various tools were used to deposit SiO₂ films, including High-Density Plasma Chemical Vapor Deposition (HDP-CVD), e-beam evaporators, and thermal oxidation. For depositing other dielectric films, we used Atomic Layer Deposition (ALD). The fabricated devices were evaluated by measuring and analyzing Capacitance-Voltage (C-V) characteristics at various frequencies. We performed 5% H_2/N_2 anneal to improve the interface trap for getting a better C-V curve. The thickness of oxide films is measured by a variable angle ellipsometer.

First, we compared the normalized C-V curves of the MOS device with SiO_2 film deposited by different tools at various frequencies (Figure 2). The C-V results are different between deposition tools, such as threshold voltage, flat-band voltage, frequency dependence. We observed the sharp transition from accumulation to inversion, so it can be said that evaporator and dry oxidation are great tools for device fabrication.

Next, we compared the normalized C-V curves of the MOS device with different dielectric films at various frequencies (Figure 3, Figure 4). The shape of C-V curves is widely different between materials. Since there is a leakage from Al_2O_3 films, we considered Al_2O3 is a bad dielectric. The C-V curves for SiO₂ and HfO₂ clearly show sharp transitions with small frequency dependence. SiO₂ and HfO₂ are great for MOS capacitors, in addition, ALD is also a great tool for fabrication.

Conclusions and Future Steps:

From the C-V curves, we conclude that e-beam evaporator, dry oxidation, and ALD are great tools for fabrication of the MOS capacitors. SiO_2 , HfO₂ are great materials for the MOS capacitor, but Al_2O_3 is a bad dielectric. For the next step, we will consider using other tools, dielectric materials, and gate electrode metals for comparison. To get better results, we will optimize some deposition conditions and measurement parameters including deposition temperature, thickness, and delay time for sweep.

Acknowledgements:

I would like to express my appreciation to my PI Dr. Lynn Rathbun, my mentors Jeremy Clark, Phil Infante, and Aaron Windsor for the advice on experimental design and useful discussion. This work is supported by National Science Foundation under Grant No. NNCI-2025233, National Nanotechnology Coordinated Infrastructure, Cornell NanoScale Science & Technology Facility, Center of Advanced Research Infrastructure for Materials and Nanotechnology of NIMS.



Figure 2: The C-V curves at 10 kHz, 20 kHz, 30 kHz, and 100 kHz for 46.84 nm SiO₂ deposited by the e-beam evaporator (red circle), 42.94 nm SiO₂ deposited by HDP-CVD (blue square), and 19.13 nm SiO₂ formed by dry oxidation (green triangle).



Figure 3: The C-V curves at 10 kHz, 20 kHz, 30 kHz, and 100 kHz for 46.84 nm SiO_2 deposited by the e-beam evaporator (red circle), 44.99 nm HfO₂ deposited by ALD (blue square), and 11.04 nm ZrO_2 deposited by ALD (green triangle).



Figure 4: The C-V curves at 10 kHz, 20 kHz, 30 kHz, and 100 kHz for 32.61 nm Al_2O_3 deposited by ALD (yellow diamond).

References:

- Houssa, Michel, et al. "Electrical properties of high-κ gate dielectrics: Challenges, current issues, and possible solutions." Materials Science and Engineering: R: Reports 51.4-6 (2006): 37-85.
- [2] Wang, Yichun, "Leakage current reduction of MOS capacitor induced by rapid thermal processing" (2010). University of Kentucky Master's Theses 640. https://uknowledge.uky.edu/ gradschool_theses/640.