Introduction by Sandip Tiwari

Presented by the CNF Technical Staff for the education of CNF Users, Potential Users, and Industrial Sponsors

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**Size Scales**

<table>
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<th>Nanometers</th>
<th>0.1</th>
<th>1</th>
<th>10</th>
<th>100</th>
<th>$10^3$</th>
<th>$10^4$</th>
<th>$10^5$</th>
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<td>Diameter of Human Hair</td>
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<td>Current feature on Microchip</td>
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<td>Quantum Mechanics Dominant</td>
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</table>

- 0.1 mm
Why nano now?

Is Nanotechnology Something New?

- Materials with nanoscale components are widespread
Is Nanotechnology Something New?

- Humans have been making systems with nanoscale components for thousands of years.
- We have been engineering materials at the nanoscale for many years.

So Why All of the Excitement?

Why Now?

Tools for seeing and manipulating structures on nanometer scales have been developed in the last 10-20 years.

Once you can see what you are doing and make changes, you can begin to do interesting work.

Why Nano?

New scientific opportunities: An unexplored world, new properties to understand.

New technologies:
- electronics, computer memory,
- bio-technology, nano-mechanical devices,
- new materials, other applications
**Information Processing**

**Predictions**

Pentium 5 linewidth = 90 nm

100,000 times improvement!

---

**Magnetic Recording**

- Three core magnetic components
  - media
  - writer
  - reader
- All require nanoscale engineering today

> 1 Gbyte hard drive

Ed Grochowski
Information Storage

![Graph showing the increase in areal density over time.](image)

Ed Grochowski

Why the NNI now?

- New discoveries, naturally nanoscale materials

- Buckyball

- Carbon nanotubes

  - Carbon Nanotube - single carbon molecule
  - Either metallic or semiconducting, depending on the pattern of rolling
  - Better thermal conductor than any other material
  - Stronger than any other material

NanoCourse Intro, page 5
The single molecule works as a transistor, but:
- Slow
- Works only at low temperatures, not room temperature
- No Gain

Now at the stage of very basic research, not close to useful technology.

Interdisciplinary: Electronic-Microfluidic
- A. Gokirmak & S. Tiwari (CNF)
A Fabrication Example: Transistors

- Lower Device: Isolation, Gate Formation, Sidewalls and Ohmic Contacts
- Bonding and layering
- Upper Device: Isolation, Gate Formation, Sidewalls and Ohmic Contacts
- Lower Device Interconnections
- Upper Device Interconnections

NanoTechnology

- Nanofabrication Processes
- Nanobiotechnology
- Nano and Microelectronics
- Optics and Optoelectronics
- Nano and Micromechanics
- Nano and Microfluidics
- Solid State Physics & Chemistry at Nanoscale
  - Magnetics
  - Ferroelectrics
  - Soft-materials
  - Quantum Structures
- Nanostructure Science
- Biophysics
- Chemical Sensors
- Molecular Scale Structures
- Self-assembled Structures
- Polymers
- Nano-Crystals

NanoCourse Intro, page 7
Wide Array of Applications

Fractionating Prism: Continuous Sorting, Austin et al.  
http://www.cnf.cornell.edu/nnun/2002NNUNreports.html


Field-Emission Displays, Simpson et al.  
http://www.cnf.cornell.edu/nnun/2002NNUNreports.html

Smallest Non-volatile Memories  

Is it all hype, or is it real?

"I know with absolute certainty that nanotechnology WILL change the world in ways it is still difficult to imagine!"

"For the long-term investor it represents a greater opportunity for profits than even the PC revolution."

"WARNING: its future is so incredible, it opens the door to a new wave of Wall Street over-hype."

Here's how to keep your feet planted firmly in the real world... and your portfolio filled with long-term nanotech winners in the most astonishing and far-reaching revolution yet.

All-New Investment Advisory from Forbes

Half-price offer!

Plus 2 Free Reports!
**A Caution**

Nanotechnology is big, but do not believe everything you read or see in popular press.

Be perceptive, use your knowledge and critical thinking.
Practical Lithography: The Art and Science of Microlithography

Optical Lithography

by

Garry J. Bordonaro

Presented by the CNF Technical Staff for the education of CNF Users, Potential Users, and Industrial Sponsors

Microlithography

Optical Lithography

Introduction
Introduction

- Optical Lithography - Mask Making
- Optical Lithography - Exposure Tool
- Optical Lithography - Techniques
- Pattern Design (CAD)

A Brief History

- The first transistor - 1947 at Bell Labs by researchers Bardeen, Brattain, and Shockley
- The first integrated circuit - 1959 at Texas Instruments by Jack Kilby.
- 1959 - Fairchild Camera, Robert Noyce - planar technology, and silicon dioxide as an insulating material on a silicon substrate.
First Transistor – Bell Labs 1947

First Integrated Circuit – Texas Instruments 1959

Courtesy Lucent Technologies

Courtesy of Texas Instruments
A layer of material such as oxide or polysilicon is grown from or deposited onto the wafer. The first material deposited helps create the first layer of the semiconductor “skyscraper.”

The photo resist, a light sensitive protective layer, is applied. The liquid photo resist is then baked to form a hardened layer that is light sensitive but resistant to chemical attack. This hardened layer acts much like the film in a camera and is used to transfer circuit images to the wafer.

A reticle with the circuit pattern for a given level is aligned over the wafer. Ultraviolet light shines through the clear portions of the reticle exposing the pattern onto the photosensitive resist.

The photo resist is chemically treated in a develop process that selectively removes the exposed regions of resist and leaves the unexposed regions containing the pattern information on the reticle.

The wafers are placed in a vacuum chamber, and a mixture of gases are pumped in and excited by electricity. This plasma eats away the material not protected by the remaining resist. When the unprotected material has been removed, the remaining material begins the pattern of the circuitry.

The remaining resist is removed in wet etch to reveal the patterned oxide layer. Then the wafer is cleaned. The process is repeated up to 18 times to create the various layers necessary for each part’s circuitry.
**State-of-the-Art Manufacturing**

90 nm Generation Interconnects

Low-k CDO Dielectric

Copper Interconnects

Combination of copper + low-k dielectric now meeting performance and manufacturing goals.

Intel

**State-of-the-Art Manufacturing**

52 Mbit SRAM Chips on 300 mm Wafer

120 billion transistors on one wafer!

These 90 nm process wafers are being routinely produced in our Hillsboro, Oregon fab.

Intel
IBM East Fishkill Wafer Fab

Market-Driven Technology

GeForce 6800
Revolutionary performance & complete Shader Model 3.0

- Complete Native Shader Model 3.0 Support
- Full support for shader model 3.0
- Vertex Texture Fetch / Long programs / Pixel Shader flow control
- Full speed 256 pixel shading
- OpenEXR High Dynamic Range Rendering
  - Floating point frame buffer blending
  - Floating point texture filtering
- Unparalleled Performance
  - 223M ops / 0.13um @ IBM
  - 6 vertex units / 16 pixel pipelines
- Next Generation Video
  - VMR / High quality compositing
  - Hardware MPEG encode / decode
  - HDTV Output
- PCI Express

Courtesy IBM
**Personal Computer Products**

Intel Xeon  
IBM Power PC

---

**Increasing Device Density**

*Figure 5: The Design Productivity Gap*

SIA Roadmap

---

Optical Lithography, page 7
Manufacture of devices depends on selective processes:

- Removal of material -- Etching
- Addition of material -- Deposition
- Modification of material -- Implantation, diffusion, etc.
**Types of Exposure**

- Light -- 436 nm - 157 nm; near UV to Deep UV optical lithography
- X-rays -- 13 nm - 0.4 nm; x-ray lithography
- Electrons -- 10 keV - 100 keV; electron beam lithography
- Ions -- 50 keV - 200 keV; focused ion beam lithography

---

**Exposure Methods**

- E-beam Dose Pattern
- Stepper Optics

---

Optical Lithography, page 9
**Resist Development**

Exposing Radiation → Resist Substrate

After Development

Positive Resist → Negative Resist

**300mm of Silicon Wafer (12”)**

Intel 300mm Wafers
**Finished Processor Die**

IBM Power PC  
Intel Pentium 4

**Lithography at CNF**

Direct Write  
CAD  
VB6  
JEOL  
DWL 66  
Nabity  

Mask Making  
PG  
DWL 66  
GCA 6100  
Suss MA6  
GCA 6300  
HTG  
GCA AS200  
EV 620  

Optical Lithography, page 11
Your Pattern Requirements

- Considerations:
  - The requirements of the lithography tool
  - The requirements of the technique you will use for the pattern transfer

Starting Suggestions

- Think about what type of design you want and how to implement it.
- Gather information from the course notes, staff members, and other students about the best tools and techniques to use before you actually sit down and design the pattern.
- Design the pattern using the information you have gathered paying careful attention to the requirements listed above.
- Perform lithography, pattern transfer, etc.
- Repeat steps 1 - 4 as many times as necessary to get it right.
To Aid the Staff (and you)

- The more thinking and preparation you do, the more intelligent the questions you ask, and the more time you end up saving the staff member.
- The more advance notice you can give about when you would like to talk about your process or be trained on equipment, the better.
- The more responsible you can be around the lab, the less we have to clean up after you, and the more time we have for answering your questions.
- And, last but not least, please be patient!

Microlithography

Optical Lithography

Mask Making
Pattern Generators

Heidelberg DWL 66

GCA/Mann 3600F

GCA/Mann 3600F Specifications

- Data input: 0.1 µm; this is the least count for object placement
- Aperture: 2 µm - 1500 µm in 0.5µm increments
- Rotation: 0 - 89.9º in 0.1º increments
- Image positioning accuracy: ± 0.6 µm over 150 mm of stage motion -- this is 4 ppm
- Aperture error:
  - ± 0.35 µm from 2 µm - 125 µm
  - ± 0.3 % from 125 µm - 425 µm
  - ± 1.25 µm from 425 µm - 1500 µm
**Heidelberg DWL66 Specifications**

- Data input: 0.01 µm; this is the least count for object placement
- Spot size: 0.6 µm with 2 mm lens; 2 µm with 10 mm lens
- Stage motion range: 200 mm
- Image positioning accuracy: ± 0.05 µm over 100 mm of stage motion -- this is 0.5 ppm
- Alignment error: +/- 100 nm

---

**PG Aperture and Positioning Errors**

<table>
<thead>
<tr>
<th>Corr (1:1)</th>
<th>4.0 µm</th>
<th>4.0 µm</th>
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<tbody>
<tr>
<td>Stepper (5:1)</td>
<td>5.0 µm</td>
<td>1.0 µm</td>
<td>7.0%</td>
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<tr>
<td>Stepper (10:1)</td>
<td>6.0 µm</td>
<td>0.6 µm</td>
<td>5.0%</td>
</tr>
</tbody>
</table>
**PG Aperture Errors**

500 µm Circle

500 µm Circle, Close up

1500 µm Circle, Close up

---

**PG 2.5, 7.5 and 10 µm Lines**

---
**PG 2.5, 7.5 and 10 μm Lines**

Out of focus and underexposed, showing abutments:

![Image of PG 2.5, 7.5 and 10 μm Lines]

---

**PG 2 μm Line Next to Large Feature**

![Image of PG 2 μm Line Next to Large Feature]
Resist Tone

Types of Glass

- Thermal coefficients for different types of glass:
  - Soda-lime: 9.3 ppm/°C
  - Borosilicate: 3.7 ppm/°C
  - Quartz: 0.5 ppm/°C
**Transmission Properties**

![Graph showing transmission properties](image)

**Other Mask-making Techniques**

- E-beam Direct-write
- GCA/Mann 6300 in Photorepeater Mode
- Outside vendors
Optical Lithography:

Exposure Tools

Hg UV Lamp Spectrum

Optical Lithography, page 21
**Contact Aligner**

![Contact Aligner Diagram]

**Contact Mask Aligners**

- Karl Suss  
  MA6
- HTG 3HR
- EVG 620
Diffraction in Optical Lithography

Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999

Diffraction in Contact Lithography

Optical Lithography, page 23
Resolution in Contact Lithography

\[ 2 b_{\text{min}} = 3 \left[ \lambda \cdot d / 2 \right]^{1/2} \]

HTG Aligner Output Spectrum

Optical Lithography, page 24
Contact Aligner Diffraction

Contact Alignment Marks

Mark on Substrate

Mark on Second Level Mask

Optical Lithography
**Contact Lithography Advantages**

- 1:1 pattern transfer means field size can be large. The HTG can expose wafers up to 4 inches in diameter using 5 inch masks, while the MA6 can expose wafers up to 6 inches in diameter using 7 inch masks.
- Substrates of various sizes and thicknesses can be used because there are no focus problems to consider.
- Substrates which have non-parallel front and back sides (wedge error) can be used because chucks on the aligners can tilt to planarize the sample.
- High resolution can be obtained in DUV mode, or mix and match lithography with e-beam resists can be performed.
- Contact lithography is easier to learn than projection.

**Contact Lithography Disadvantages**

- Good contact is difficult to achieve because of particulates between mask and substrate, and flatness variations.
- As a result of particulate contamination, defects are more numerous than in projection lithography.
- Small geometries (< 2 µm) require a mask made on an e-beam system.
- DUV exposures require a quartz mask.
- Alignment can be time consuming and is not very accurate (especially if the scheme for marks has not been well thought out).
**Stepper Optics**

- Mirror
- Hg Arc Lamp
- Filter
- Condenser Lens
- Mask (4-10x) Of Chip

**248nm Excimer Laser Spectrum**

![Graph showing the typical spectrum of an ELS-6010 laser system with FWHM of 0.32 pm, 195% of 0.97 pm, and an energy of 6.5 mJ.]

*Courtesy of Cymer, Inc.*

Optical Lithography, page 27
Excimer Laser Schematic

Stepper Diffraction

\[ \sin \theta = \frac{N \lambda}{d} \]
Diffraction in a Grating

Diffraction Orders

Pupil
Objective Projection Lens
Mask (Aperture)
Wafer Image Plane

Diffracted Order Spread

Diffracted Light Waves
Plane Light Waves
Screen

Intensity vs. Angle

\( b = 5\lambda \)

\( b = 2\lambda \)
**Lens Collection of Diffracted Orders**

Minimum condition for imaging - more than 0th order

Collection lens

Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999

---

**Diffracted Order Filtering**

0, +/-1, +/-2, +/-3 orders  Resulting dense line image

0, +/-1 orders only  Loss in image modulation

Biased cosine function

Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999
Optical Lithography Limits

- Minimum Feature Size
  - \( d_{\text{min}} = \frac{k \lambda}{\text{NA}} \)

- Depth of Focus
  - \( D = \frac{k \lambda}{2 \text{(NA)}^2} \)

Aerial Image vs. Wavelength
Aerial Image vs. Numerical Aperture

Aerial Image vs. Focus

Optical Lithography, page 33
GCA Wafer Steppers

GCA 6300 5X or 10X

GCA Autostep 200

CNF Stepper Characteristics

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Optical Lithography, page 34
GCA Wafer Alignment

![GCA Wafer Alignment Diagram]

Projection Lithography Advantages

- Resolution comparable to the best contact lithography with no degradation of mask or resist.
- More tolerant of mask errors since mask image is reduced in size on the substrate. Almost all masks can be made on the PG.
- Step and repeat means many exposures per wafer, with the flexibility of computer control.
- Better alignment accuracy, typically ± 0.25 µm for the older GCA steppers.
**Projection Lithography Disadvantages**

- Focus requirement means that substrate thickness is limited, as well as wedge error (newer steppers have leveling).
- Field size is limited.
- More complicated to learn than contact lithography.

**Lithography Considerations**

- Your pattern requirements:
  - Pattern size, feature size, alignment accuracy
- The requirements of the lithography tool:
  - Field size, mask size, mask type, alignment marks
- The requirements of the technique you will use for the pattern transfer:
  - Mask tone, resist type, resist thickness
Optical Lithography: Techniques

Industrial Progress

AND HIGH VOLUME PRODUCTION
(Past Performance and Future Projections)

HALF PITCH MINIMUM FEATURE SIZE (MICRONS)

YEAR
Moore’s Law Continues

Figure 7: ITRS Roadmap Acceleration Continues—Half Pitch Trends

Pentium 4 Die

Intel Corp.
Photoresist Components

- Novolak Resin
- DNQ Photosensitizer

DNQ - Indene Carboxylic Acid

- Moreau, p. 35
**Resist Absorbence Curve**

Shipley Product Information

**Poor Resist Profile**

2.0 µm lines and spaces in 1.0 µm Shipley 1400 resist, exposed with the 10:1 i-line stepper
**Correct Resist Profile**

0.7 µm lines and spaces in 1.0 µm thick OCG 895i resist, exposed with the 10:1 i-line stepper

**Silicon Surface Hydration**

Shipley Tutorial Graphics
**Primming with HMDS**


---

**Resist Spin Speed Curve**

OCG Process Application Note
Standing Wave Effects

Calculated

No PEB

PEB, 115°C, 45 sec.

Dammel, p. 110.

Standing Waves

Optical Lithography, page 44
Resist Profile After Postbake

Resist Processing

- Development
  - PEB
  - 300MIF, MF-321, MDC
  - Hardbake

- Stripping
  - Hot Strip Bath
  - 1165 Remover
  - O2 Plasma
Positive Tone Process

Exposure

Development

Etching

Positive Tone Sidewall Slope

- After Development

- After Metalization
**Lift-off Using Image Reversal**

Exposure

Mask

Resist

Substrate

Reversal

Development

Evaporation

---

**Lift-off Process**

- After Image Reversal

- After Metalization

---

Optical Lithography, page 47
Image Reversal

Image Reversed Resist Profile
Summary of Considerations

- Your pattern requirements:
  - Pattern size, feature size, alignment accuracy

- The requirements of the lithography tool:
  - Field size, mask size, mask type, alignment marks

- The requirements of the technique you will use for the pattern transfer:
  - Mask tone, resist type, resist thickness

8” Intel Wafer

![8” Intel Wafer Image]
Pattern Layout and Translation...

This part of the process is where you take what you think you want, and put it into a form that the instruments at the CNF will understand.

Typically, this starts with CAD, which uses lines, equations, polygons, algorithms, rectangles, etc…
**Pattern Layout and Translation**

... to create your pattern:

![Pattern Layout](image)

**The Process**

- Draw your structure
- Convert your pattern to machine-specific data
- **Check the result!**
  - Is the data correct?
  - Is the data reasonable (usually exposure time)?
- Expose your pattern

This is an evolutionary process!
Some Terms

- **GDS** – industry standard format for the exchange of layout data. (aka GDS-II, aka STREAM).
- **User Units** – what the user sees as the units used for their patterns. Usually in microns. (Not the lower limit of what you can use.)
- **Internal Units** – how User Units are defined internally. Usually expressed as 1000 Internal Units per User Unit (1 nanometer).
- **Datatype** – mechanism for a user to optionally associate data with a particular object. At the CNF, most commonly used to provide exposure hints for e-beam patterns.
- **CIF** – another exchange format.
- **DXF** – AutoCAD text exchange format. We can read DXF. AutoCAD can be used for nanofabrication patterns, but there are better solutions.
**Some More Terms**

- **Alignment Marks** – Special sets of shapes that are used to align subsequent processing steps.
  - First part would be included during an exposure.
  - The second part would be included in the next exposure, to match up with the mark already on the wafer.
  - For additional exposures, you may need additional marks.

- **Fracture** – related to the process where your shapes are broken into much smaller shapes that the tool can expose.
  - **Mann PG** – Overlapping, rotated rectangles (2 µm to 1500 µm, in _µm steps).
  - **E-Beam** – Quadrilaterals, and single-pass lines. Generally, overlaps are removed. Overlapping figures can be used to fine-tune an exposure.

---

**Circles, and other curved figures ...**

... are supported by some CAD tools, BUT

- NOT by GDS, and
- NOT by the lithography tools.

Instead, they will be approximated by regular polygons, or a series of line segments. You control the accuracy of the approximation.

A more accurate approximation will usually take more time, more space, and more money.

The question to ask is:

“What is good enough?”
Layers

Lithography is a 2-D exposure that, after additional processing, results in a 3-D structure. **Layers** are the mechanism in CAD used to identify these exposure steps.

- Usually, a layer in CAD will translate to a single exposure (or mask).
- In some cases, it is useful to use multiple layers for a single exposure.
- There may be other layers, for additional information, layout guides, or tone-reversal.
- Layer definitions apply to all of the cells in a layout or library. However, a cell will typically not use all of these layers.

Cell

A **cell** is the basic building block of your pattern.
**Cells**

A cell can refer to other cell(s).

A cell can also refer to an array of another cell.

Any subsequent changes to the child cell will propagate.

Copy/Paste of the contents of one cell to another will **NOT** maintain this linkage, usually resulting in confusion and/or extra work.

---

**Layout / Library**

A **layout** (or **library**) is a collection of one or more cells, with one or more layers defined, plus some other information.

For very complex structures, one structure per layout.

At the CNF, people will often have multiple structures in a single layout, but this is a personal choice, and not a technical one.
**Where do I want to be?**

- Draw your structures actual size. The tool ultimately used to expose your pattern isn’t significant at this time. This leaves your options open.
  - Any tool-specific scaling will be done during conversion.
  - The output of the conversion process is instrument-specific, the output of CAD is not.
  - Tone-reversal is usually done during conversion.

- **However**, some things **ARE** tool-specific…
  - Positional accuracy.
  - Alignment marks.
  - Performance characteristics.
  - ...

---

**I want to be where?**

Size matters. Distances matter.

(-9.9843, 6.3421)  
???

But, location also matters!
But I was over there, wasn't I?

MANN PG Design Issues - Angles

Right (90°) and Obtuse (>90°) fracture easily:

2 Flashes

3 Flashes
While Acute ( < 90° ) tend to suffer data explosion:

More sides on your circle mean more flashes on the PG.
MANN PG Design Issues - ‘Circles’

4 Flashes

80 sides result in 64 flashes
(r = 100 µm)
MANN PG Design Issues - ‘Circles’

It gets even worse once you exceed the aperture size

4 sides result in 9 flashes

80 sides result in 1052 flashes
\((r = 3000 \, \mu m)\)
MANN PG Overlap Removal

As Designed:

As Interpreted:

As Converted:
(27 flashes)

Layer A

Layer B

A Solution:

CAD, page 12
E-Beam Design Issues

- The maximum area that the electron beam can trace at one time is called an exposure FIELD.
- A pattern larger than this field will require stage motion.
- The intersections between fields are called STITCHING LINES.
- STITCHING ERRORS occur along these lines.
- Therefore, keep small features in the center of the field!

GDS Issues

- GDS is a binary format – if you are using FTP (or similar) to transfer, make sure that it transfers as Binary (or Image).
- There are various flavors of the GDS specification. There are also ‘enhancements’ that various companies made.
  - Uppercase cell names are easier. (For instance, L-Edit has an export option that will do this for you.)
  - Some software will generate polygons with thousands of vertices. 200 or less works much better.
Practical Lithography: The Art and Science of Microlithography

Electron Beam Lithography
by
Alan Bleier

Presented by the CNF Technical Staff for the education of CNF Users, Potential Users, and Industrial Sponsors

Topics Covered

- Why use e beams for lithography?
  - Examples of research done with EBL
- A little physics
- Practical description of using e beams
  - in the order you would actually do things
- CNF e-beam systems
**What is Electron Beam Lithography?**

- Focused beam of electrons
- Computer driven pattern generator
- Serially expose individual points to create a pattern (direct write)
- Alternatively, expose rectangular or triangular patches (shaped beam) or project sections of a pattern (e.g. PREVAIL, SCALPEL)
- Irradiation causes chemical change in resist
- Latent image developed by selective solution

---

**Why Use Electron Beams?**

<table>
<thead>
<tr>
<th>Optical Lithography</th>
<th>e-Beam Lithography</th>
</tr>
</thead>
<tbody>
<tr>
<td>High speed for large shapes</td>
<td>High speed for complex Patterns</td>
</tr>
<tr>
<td>High Speed, Parallel Exposure</td>
<td>Point by Point Exposure Limits Speed</td>
</tr>
<tr>
<td>Light Diffraction Limits</td>
<td>Not Diffraction-limited;</td>
</tr>
<tr>
<td>Minimum Feature Size to 50 nm at best</td>
<td>Resolution 20 nm</td>
</tr>
</tbody>
</table>
Diffraction Error


Resolution Limited by Sum of Aberrations

History of SEM and e-Beam Lithography

- 1926 H. Busch (Berlin) – Theory of electron trajectories
- 1939 Knoll & Theile (Berlin) – First SEM, 100 µm spot
- 1939 von Ardenne (Berlin) – First good SEM, 0.1 µm spot
- 1948 C. W. Oatley & D. McMullan (Cambridge) – First modern SEM using two scan coils and secondary electron collector
- 1965 IBM, Cambridge, Hughes experiments with first beam writing using pump oil contamination and low-resolution Kodak resists
- 1971 M. Hatzakis, A. Broers, E. Wolf – PMMA for 60 nm lines
- 1974 EBES (Bell Labs) commercial e beam system, later spun off to Perkin Elmer
- 1985 National Nanofabrication Facility purchases JEOL JBX5DII

Examples
**e-Beam Process Example**

- Lithography and Pattern Transfer

![Diagram showing the process steps: resist substrate, expose and develop, evaporate metal, soak in acetone to lift off metal, plasma or wet etch, strip resist.]

**Example Mixed Optical & e-Beam: GaAs FET**

- Mesa isolation
- Ohmic metal and alloy
- Gate lith. & recess etch
- Evap. gate metal & liftoff
- Large bond pads
Research Done With Nality NPGS on LEO SEM

- Dual Exposure Glass Layer Suspended Structures (DEGLaSS)
- David Tanenbaum (Pomona College)
- Anatoli Olkhovets and Lidija Sekaric (Cornell)
- Amorphous Glass, Hydrogen Silsesquioxane (HSQ).

- 1 - 3 keV for suspended layers
- 3 - 20 keV for support structures

Research Conducted With Leica EBMF

IR Crossed Dipole Resonant Filter
Glenn Boreman group (U. of Central Florida)
Infrared Antennas

- Glenn Boreman group (U. of Central Florida)
- ~ 200 nm Al leads
- Nb bolometer

Photonic Crystal Microcavity InP-based Devices

- Jayshri Sabarinathan, Pallab Bhattacharya (U. of Michigan)
- EBMF writes the reverse of the pattern on oxide (on top of InP/GaAs device). Then using dry etch and liftoff, reverse the pattern. Etched in the ECR tool
- Minimum feature sizes from 100 to 200 nm
Disordered Superconducting Networks

- Yi Xiao (Princeton University)
- 1 mm Kagome structure with random defects
- 180 nm wide wires 50 nm Al liftoff array, 50 nm Au liftoff leads and contacts

Addressable Carbon Nanotube Arrays

- Joel Moser, Michael Naughton (Boston College)
- Array of 40 nm Ni dots on platinum leads for carbon fiber growth and molecular attachment
Addressable Carbon Nanotube Arrays

- ATM Image
- Patterned on Leica VB6
- Small dots made with aligned second exposure

Joel Moser, Michael Naughton (Boston College)

Carbon Nanofibers for Field Emission Devices

- Michael Guillorn, Michael Simpson (U. Tennessee, Knoxville)
- Arrays of programmable e− emitters made of vertically-aligned carbon nanofibers (VANCF)
- 50 nm dots on 50 nm pitch, drawn as 40 nm octagons
- Fibers grown by e gun PVD
Hyuncheol Koo, R. D. Gomez (U. of Maryland)

- Island size 300 nm by 900 nm
- Magnetic dipole at the ends of island - dark and bright
- The neighboring island produces stray field which may change the switching characteristics of islands

Two Au electrodes exposed in two separate steps
- Second electrode aligned to the first using the VB6
- By changing the offset between the electrodes, can typically obtain sub-10 nm gaps
Physics of Atomic-Scale Conducting Objects

- Dragomir Davidovic (Georgia Inst. of Technology)
- Investigates electron transport in atomic-scale diameter contacts between metals and single molecules bridging atomic scale gaps between metals

Studying Organic Semiconductor Molecules

- Yuanjia Zhang, George Malliaris (Cornell)
- 27 nm gap between electrodes
**Nanomechanical Resonant Systems**

- Harold G. Craighead group / Dustin Carr (Cornell)
- Released silicon
- 50 nm strings on “harp”

**Nanomechanical Resonant Systems / NEMS**

- Harold G. Craighead Group / Lidija Sekaric, Keith Aubin, Jingqing Huang (Cornell)
- 6 to 12 µm long Si strings, 150 to 200 nm wide
- Focused laser beam excites oscillations in strings
- Possible applications - low power mechanical oscillators & filters
A Little Physics

Electron-solid interactions

- Forward scattering
- Backscattering
**Secondary electrons**

- Much of primary electron energy is dissipated in the form of secondary electrons with energies from 2 to 50 eV
- Responsible for the bulk of the actual resist exposure process
- Range in resist is only a few nanometers
  - Contribute little to the proximity effect
- Net result is effective widening of the beam by roughly 10 nm
- Main reason for minimum practical resolution of 20 nm in the highest resolution electron beam systems
- Contributes (along with forward scattering) to the bias that is seen in positive resist systems, where the exposed features develop larger than the size they were nominally written.
Modeling


Proximity effect

Proximity Effect – Inter- and Intra- 

Primitive proximity effect correction by assigning dose clocks to features of different sizes 

Conditional Feature Assignment with CATS
Using e-Beams
- in the order you would actually do things

**e-Beam Lithography Procedure**

- Design Pattern with CAD
  - Convert Pattern to Machine Format
- Choose Resist and Apply to Sample
- Expose
- Develop
**Background for CAD - Beam Scan Basics**

Bojko, Richard, CNF EBMF Manual, [www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html](http://www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html)

---

**Pattern Writing Strategies**

- Vector Scan
- Raster Scan
- Shaped Beam
Two Dimensional e-Beam Field

Vector Scan to Fill In Shapes

Fracturing Shapes


Hierarchy of Pattern Exposure Elements

- Wafer – an array of chips or dies
- Die or chip – one or more fields

**Fields and Subfields**

- Chip
- Field
- Subfield

**Registration**

- Wafer
- Chip or die with alignment marks


E Beam, page 21
**Resolution, Current and Dose Issues**

- Dose is charge/area, $\mu$C/cm$^2$

$$D = \frac{I \times t}{A} = \frac{I}{A \times f}$$

- $I$ = current, typically 1, 2, 5, 10, 20, 50 nA
- $A$ = area for a single beam step, e.g. 5 nm x 5 nm
- $f$ = clock frequency
- Higher current -> faster write time, but lower resolution
- Stage moves (~ 1 s) may be major contributor to exposure time

---

**Variable Resolution Unit (VRU) table**

- VRU is a multiple of smallest beam step size
- CFREQ command on VB6 calculates clock frequency, current, dose or exel (beam step) size
- Trade off current and beam step size to get high resolution and fast write time with less than max. clock frequency

<table>
<thead>
<tr>
<th>VRU</th>
<th>Beam Step Size, nm</th>
<th>Min. Dose, uC/cm$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>160</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>4</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>40</td>
<td>2.5</td>
</tr>
<tr>
<td>16</td>
<td>80</td>
<td>0.63</td>
</tr>
<tr>
<td>32</td>
<td>160</td>
<td>0.16</td>
</tr>
</tbody>
</table>
**Coordinate Systems / Stage Mapping Modes**

- Global / Wafer
- Die / Chip
- Field within chip

**General Guidelines for Pattern Layout**

- Design for e-Beam exposure
- Use a design grid

Bojko, Richard, CNF EBMF Manual, [www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.5.html](http://www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.5.html) and [www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html](http://www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html)
### Populated Grid

- No field stitching except in BigDevice which is larger than one field

![Populated Grid Diagram](image)

Bojko, Richard, CNF EBMF Manual, [www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html](www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html)

### Combining e-Beam with Other Types of Lithography

- Alignment accuracy ~ 10 nm is achievable
- Techniques that make alignment marks visible (to your eye and to the machine) in a 100 keV scanning electron beam include
  - Specific shapes
    - Squares or octagons with 4-50 μm sides
  - Materials
    - 1 μm-deep etched pits in Si
    - 50 - 100 nm of Au, Pt, W liftoff metal (high atomic number difference between mark and substrate)
    - Al doesn’t work on Si or GaAs substrates

![Combining e-Beam Diagram](image)
Making and Positioning Marks

- Global marks
  - 3 widely spaced marks such as GCA key

Locating Marks

- Global Alignment or Wafer Alignment


Local or Field Alignment

- Typical 4 mark field

![Image of typical 4 mark field](210 \mu m)


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Basic Mechanisms of Alignment

- Simple image processing
- Coarse and fine scanning

![Image of basic mechanisms of alignment](2.4 \mu m + 1.2 \mu m)

**Easy Mark**

- Hi Z contrast between Au mark on Si, no resist
- 4 µm wide mark, 80 pixels wide

![Image of Easy Mark graph]


**Difficult Mark**

- 400 nm Tantalum on Si, buried under 100 nm thick SiO₂ film
- Only topographic edge contrast seen
- Noise from roughness of tantalum surface

![Image of Difficult Mark graph]

**Mark Parameters**

- Schematic line scan of a pit type alignment mark scan on EBMF

![Diagram](image-url)


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**Multi-field Die Alignment**

- Field by Field Alignment

![Diagram](image-url)


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E Beam, page 28
## Resists and Processing

- Positive resists
  - PMMA
  - Toray EBR-9
  - PBS
  - ZEP
  - Photoresists as e-beam resists
- Negative resists
  - COP
  - Shipley SAL
  - NEB-31
- Multilayer systems
  - Low/high molecular weight PMMA
  - PMMA/copolymer
  - Trilayer systems

## Poly(methyl methacrylate) (PMMA)

- The most popular e-Beam resist
- Extremely high-resolution
- Easy handling
- Excellent film characteristics
- Wide process latitude
- Usually dissolved in a solvent (e.g. anisole)
- Exposure causes scission of the polymer chains
- Solvent developer dissolves exposed (lighter molecular weight) resist
PMMA Characteristics

- Positive acting
- Several viscosities available, allowing a wide range of resist thickness
- Not sensitive to white light
- Developer mixtures can be adjusted to control contrast and profile
- Appropriate processing results in undercut profile for liftoff
- Poor dry etch resistance
- No shelf life or film life issues

PMMA Basic Processing

- Surface Preparation
  - In general, no surface preparation (aside from normal cleaning) is necessary. Excellent adhesion to most surfaces
- Spin
  - Speed 1000-5000 rpm, 60 sec. (100-1000 nm)
- Pre-bake
  - 170 deg C oven, 1 hr. Non-critical. Must be $150 < T < 200$ degrees, for at least 30 minutes. May also be hot-plate baked
- Expose
  - Dose around $100 \mu C/cm^2$ at 20 kV
Spin-Speed Characteristics for PMMA, 495K

- Thicker films

- Thinner films


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**P(MMA-MAA) Copolymer Resist**

- Higher sensitivity than PMMA
  - Can be exposed at a lower dose
  - Faster
  - Less contrast
- Most useful in Bi-level resists with PMMA, to produce undercut profiles useful in liftoff processing
- Characteristics
  - Positive acting
  - Several viscosities available, allowing a wide range of resist thickness
  - Not sensitive to white light
  - Developer mixtures can be adjusted to control contrast and profile
  - Poor dry etch resistance
  - No shelf life or film life issues

---

**Tour through an e Beam Lithography Column**

- Leica Microsystems Lithography, Ltd. VB6
**Electron Source - Tungsten and LaB₆ Gun**

- Example: Leica Microsystems Lithography EBMF


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**Electron Gun**

- Wehnelt and Gun Crossover – W and LaB₆


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E Beam, page 33
**Electron Source – Thermal Field Emitter (TFE)**

- Example: Leica Microsystems Lithography VB6

![Diagram of TFE electron source](image)


---

**Comparison of Electron Sources**

<table>
<thead>
<tr>
<th>Source Type</th>
<th>Brightness</th>
<th>Lifetime</th>
<th>Source Size</th>
<th>Energy Spread ΔE</th>
<th>Beam Current Stability</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tungsten</td>
<td>10³ A/cm²sr</td>
<td>400-1000 h</td>
<td>60-100 μm</td>
<td>1-3 eV</td>
<td>1%</td>
<td>[6]</td>
</tr>
<tr>
<td>Field Emission</td>
<td></td>
<td></td>
<td>5-50 nm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cold</td>
<td>10⁶</td>
<td>&gt;10000</td>
<td>&lt;5 nm</td>
<td>0.3</td>
<td>5%</td>
<td>[5]</td>
</tr>
<tr>
<td>Thermal</td>
<td>10⁸</td>
<td>&gt;10000</td>
<td>&lt;5 nm</td>
<td>1</td>
<td>5%</td>
<td>[5]</td>
</tr>
<tr>
<td>Schottky</td>
<td>10⁵</td>
<td>&gt;10000</td>
<td>15-30 nm</td>
<td>0.3-1.0</td>
<td>2%</td>
<td>[5]</td>
</tr>
</tbody>
</table>


---

E Beam, page 34
**Electron Optics – Magnetic Electron Lens**

- Copper windings
- Iron shell
- Polepieces
- Electron optic axis

**Magnetic Electron Lens**

- \( u = \text{Object Distance} \)
- \( v = \text{Image Distance} \)
- \( f = \text{Lens Focal Length} \)

Magnification: \( m = \frac{v}{u} \)

Simple Lens Equation: \( \frac{1}{u} + \frac{1}{v} = \frac{1}{f} \)


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Electrostatic Lens


Other Electron Optical Elements

- Beam blanking
- Stigmators
- Electron beam deflection
- Apertures
Beam Blanking

- Turning the beam on and off
- Usually accomplished with a pair of plates set up as an electrostatic deflector
- One or both of the plates are connected to a blanking amplifier with a fast response time
- Voltage applied across plates sweeps beam off axis until it is intercepted by a downstream aperture

Conjugate blanking
- Beam at target does not move while the blanking plates are activated
- Prevents leaving streaks in the resist as beam is blanked
- Blanking plates are centered at an intermediate focal point, or crossover

Deflector and Stigmator

**Beam Deflector**

![Beam Deflector Diagram]


---

**Final Aperture**

- Measured beam diameters at 20 kV
- Smaller final aperture does not always produce smaller beam

![Final Aperture Graph]

Dynamic Corrections for Aberrations

- Example: deflection-induced beam defocusing


Stage Enables sub-100 nm Lithography

- Stage has laser interferometer with $\lambda/1024 = 0.6$ nm precision
- Beam Error Feedback (BEF) corrects for stage position and vibration in real time

Mapping Distortions to Correct Them

- Five coefficients parameterize distortion correction
  - Rotation Angle
  - X scaling
  - Y scaling
  - X translation
  - Y translation


Height Mapping to Minimize Stitching Errors

- Real time laser height sensor for dynamic correction of field size, focus, astigmatism

Typical Exposure Sequence

- Ready the airlock for venting
- Vent the airlock
- Load the wafer into a chuck
- Load the chuck into the airlock
- Pump the airlock back to vacuum
- Load and settle the chuck on the exposure stage
- Set up the machine operating parameters
- Run your exposure job file
- Unload chuck
- Remove the chuck from the airlock

PMMA Basic Processing – post exposure

- Develop
  - 1:1 MIBK:IPA, 1-2 minutes
- Rinse with IPA
- Dry by spinning or dry N₂
- Post-Bake not normally necessary
- Light Descum
- Stripping
  - Acetone will strip PMMA
  - NMP (Remover 1165)
  - Strong bases (KOH)
  - Acid normally hostile to organics, such as NanoStrip
  - Oxygen plasmas etch PMMA very well
CNF e-Beam Systems

CNF has 3 complementary systems

1. Nabity Nanometer Pattern Generation System (NPGS) on LEO SEM
2. Leica VB6 HR
3. JEOL 9300FS
**Nabity Nanometer Pattern Generation System (NPGS)**

- PC-based pattern generator
- Interfaced to a LEO 982 scanning electron microscope
- 1 to 30 keV

David Tanenbaum
(Pomona College)

---

**Leica VB6-HR**

- For features from above 1 µm to below 30 nm
- Thermal Field Emission electron source running at 100 kV provides high brightness and small source size
- Minimum feature sizes < 30 nm are possible
- Field sizes up to 655 µm
- Beam currents as high as 50 nA
- Flexible job control language
JEOL 9300FS

- General purpose high-resolution electron-beam lithography
- Thermal Field Emitter electron source at 100 kV
- Beam spot size 4 nm
- Repeatable minimum resolution < 20 nm
- Pixel step 1 nm
- Placement and automated alignment accuracies of 20 nm over a 0.5 mm field
- Max 25 MHz clock, 20-bit pattern generator
- Wafers and masks up to 12 inches
- Upgrades to 50 MHz clock and 1 mm field size in future

References and Acknowledgements

- Leica Microsystems Lithography, Ltd.