Improving Dopant Activation in III-V Materials using LSA

CNF Project Number: 150-82

Principal Investigators: Michael Thompson, Paulette Clancy

Users: Hsien-Lien Huang, Emily R. Cheng, Victoria C. Sorg

Abstract:

The high temperatures and short annealing times (sub-millisecond to millisecond) of laser spike annealing (LSA) have the potential to increase activation of ion-implanted compound semiconductors to levels necessary for use in future generations of CMOS technology as well as power electronics. These conditions enable access to both metastable activation levels after ion implantation, and extended process temperatures without deactivation from in situ doped metastable films. Single stripe LSA scans were conducted to probe thermal damage behavior and electrical characteristics as a function of peak annealing temperature and heating dwell.

Summary of Research:

As silicon transistor technology is pushing material limits, major scaling challenges remain. Ultimately, a shift towards a new device architectures and geometries are needed, but a possible short-term solution to continue scaling is to replace silicon with materials that are better suited for a particular device. Compound semiconductors are strong candidates, e.g. In$_{0.53}$Ga$_{0.47}$As (InGaAs) for low power, n-type materials for transistor channels and source/drain contacts and GaN for power electronics for high temperature and voltage applications. However, challenges arise when attempting to maximize dopant activation during thermal processing due to thermal budget limitations.

In this project, sub-millisecond and millisecond (sub-ms to ms) LSA was investigated as a method to improve the activation of ion-implanted dopants and to limit deactivation of grown-in dopants in InGaAs and GaN. LSA uses a continuous-wave, line focused laser scanned over a sample to rapidly heat and quench samples (rates of 10$^6$ K/s and 10$^5$ K/s, respectively). Using spatially resolved measurements perpendicular to the single laser annealing scan, a continuous range of annealing temperatures can be tested from room temperature to the highest annealing temperature reached [1]. Two types of samples were used to study the laser annealing damage threshold and dopant behavior with LSA; ion-implanted and molecular beam epitaxy (MBE) grown samples (either unintentionally doped and intentionally doped).

The thermal processing limits and peak laser annealing temperature calibration was determined for gallium nitride (GaN) using the known thermal decomposition behavior of a polymer and melting behavior of gold dots. The polymer decomposition served as a rough estimate for peak annealing temperatures, which were then further explored by using the melting of gold dots. The GaN samples were annealed using a 10.6 µm wavelength CO$_2$ laser.

A block copolymer (poly(styrene-block-methyl methacrylate), 70 wt.% polystyrene), with complete thermal decomposition of 850°C, was spun to a thickness of 60 nm on GaN samples (GaN-on-GaN or GaN-on-sapphire) and laser annealed at power conditions ranging from 32-56 W, all with 1 ms dwells. The peak temperature GaN reached before thermally induced damage was established to be in the 1400-1600°C range for GaN-on-sapphire.

After obtaining approximate peak annealing temperatures from the polymer decomposition experiment, more specific temperature calibrations were achieved...
using the gold dot method. Gold dots with diameters on the order of 2-5 µm were fabricated using photolithography using a standard liftoff procedure. A 50 nm SiN₃ layer was deposited on the GaN substrates using Oxford plasma enhanced chemical vapor deposition (PECVD) (to limit N evaporation at high annealing temperatures). The dots were photolithographically patterned and metal was deposited using thermally evaporated chrome (10 nm for adhesion) and gold (25 nm). The samples with gold dots were laser annealed at conditions ranging from 10-30 W with a 1 ms dwell. An example annealed stripe is shown in Figure 1. Results from the gold dot experiment show the samples reaching temperatures above the gold melt threshold (1064°C).

To gain a better understanding of the laser annealing damage behavior of GaN on sapphire substrates, a sapphire sample was laser annealed. The sapphire (Al₂O₃) substrate was prepared by removing silicon thin film layer from a silicon-on-sapphire sample by etching with a 50% KOH solution for three minutes at 80°C. A CO₂ laser was scanned with a 1 ms dwell, at 22.5 W. The resulting laser annealing damage has a crosshatch texture shown in Figure 2. The crystalline slip damage along the annealing direction is most likely the result of the combination of poor thermal conductivity compared to other candidates (Si:150, GaN:130, InP:68, Al₂O₃:23.1 W/m·K), and high light absorbance of sapphire with thermally-induced strain that causes damage before reaching the melting point of sapphire at 2050°C.

The dopant activation behavior of laser annealed, ion-implanted, thin InGaAs film on an InP substrate was explored for ultra-shallow junction applications. A 20 nm InGaAs thin film was ion-implanted with silicon and capped with 3 nm Al₂O₃ layer to prevent arsenic evaporation at high temperatures. The sample was annealed with a 980 nm diode laser with a 5 ms dwell at 75 Amps. Based on the decomposition behavior of the polymer, the sample reached a peak temperature of 1060°C before it cracked (Figure 3), likely due to InP melting point based on previous annealing results.

Overall, the damage threshold and peak temperatures reached during laser annealing of compound semiconductors was explored. These studies set the basis for future annealing studies and characterization of how electrical properties are affected by annealing time and temperature.

**References:**

Vector Electric field Measurements Using Position-Modulated Kelvin Probe Force Microscopy

CNF Project Number: 863-00
Principal Investigator: Prof. John Marohn
Users: Ryan Dwyer, Ali Tirmzi

Affiliation: Department of Chemistry and Chemical Biology, Cornell University
Primary Source of Research Funding: National Science Foundation, Division of Materials Research (NSF-DMR 1006633)
Contact: jam99@cornell.edu, rpd78@cornell.edu, st759@cornell.edu
Website: marohn.chem.cornell.edu
Primary CNF Tools Used: MOS thermal oxidation furnace, SC4500 evaporator, Autostep i-line stepper

Abstract:

High-quality local measurements of electric fields are critical to understanding charge injection, charge transport, and charge trapping in semiconducting materials. Here, we report a new variation of frequency-modulated Kelvin probe force microscopy that enables local measurements of electric field along multiple directions simultaneously by employing position modulation and lock-in detection instead of numeric differentiation of the surface potential. This technique is simple to implement and should be especially useful for studying electric fields in spatially inhomogeneous samples like organic transistors and photovoltaic blends. We demonstrate the technique on a organic field-effect transistor (bottom-gate, bottom-contact) made from the hole-transporting small molecule DPh-BTBT.

Summary of Research:

We report a simple modification of frequency-modulated Kelvin force microscopy (FM-KPFM) that enables the direct spatial imaging of electric fields near a surface along multiple directions simultaneously. The lateral electric field in a FM-KPFM measurement is typically obtained by numerically differentiating the measured surface potential versus position to obtain a plot of electric field versus position [1-3]. This microscopically measured electric field can be helpful for understanding both device physics and materials properties.

Many KPFM measurements derive information mainly from contrast in surface potential images or the average difference in surface potential over different regions of the sample. These properties are relatively insensitive to feedback loop dynamics, noise and surface potential fluctuations. In contrast, these sources of error affect the calculated electric field dramatically. If the scan speed is carefully optimized, low-frequency surface potential noise along the scan axis can be avoided without distorting the measured electric field significantly. In a 2D raster scan, however, the electric field measured along the slow-scan axis will still be subject to large low-frequency surface potential noise caused by position hysteresis and surface potential fluctuations.

To avoid this low-frequency noise, we modify the FM-KPFM measurement by adding a small position modulation δr. We use a modulation δr(t) = A _pm sin(2πf _pm t) with A _pm the modulation amplitude and f _pm the modulation frequency. We detect the electric field as an oscillating potential at the modulation frequency with amplitude A _pm E _pm. We call the technique position-modulated Kelvin probe force microscopy (PM-KPFM).

To calculate the electric field from the position-modulation signal, we processed the raw surface potential data using a software lock-in amplifier at the position-modulation frequency f _pm = 4.5 Hz. We used a 0.8 Hz bandwidth lock-in amplifier filter. The measured electric field is E _pm = X _LI /A _pm, where X _LI is the in-phase channel of the phased lock-in amplifier output.

Figure 1 shows our DPh-BTBT thin-film transistor. To fabricate the transistor, we evaporated 100 nm of DPh-BTBT onto a transistor substrate. The transistor substrate was a highly n-doped silicon gate, a 300 nm thermally grown silicon oxide insulator layer (wet oxide deposited using MOS thermal oxidation furnace), and 40 nm thick thermally evaporated gold source and drain electrodes (SC4500 evaporator, Autostep i-line Stepper). The channel width was 5 µm.
Figures 2 and 3 demonstrate using PM-KPFM to measure the electric field along the slow-scan axis more precisely. We collected a KPFM image over the DPh-BTBT transistor with source, gate, and drain electrodes off (Figure 2). The KPFM image revealed pockets of trapped charge in the transistor channel.

To probe the electric field near these trapped charges, we took a PM-KPFM linescan. We applied the position modulation perpendicular to the scan direction so that we simultaneously measured $E_x$, the electric field along the fast-scan direction, and $E_y$, the electric field along the slow-scan direction. The electric field $E_y$ was determined by numerically differentiating the measured surface potential with respect to the fast-scan direction while $E_x$ was obtained from XLI as discussed above. Figure 3 shows the KPFM image contours along with the in-plane electric field vector ($E_x, E_y$) measured by PM-KPFM. One consequence of the electric field being the negative gradient of the electrostatic potential is that the electric field vector at location $\mathbf{r}$ must be perpendicular to a line tangent to the constant-\(\phi(x, y)\) surface passing through $\mathbf{r}$. This perpendicular relationship is clearly evident in Figure 3, demonstrating PM-KPFM's ability to serve as a vector electrometer.

We anticipate that the simple modification of FM-KPFM introduced here will be useful for electric field measurements in a variety of systems. Although we demonstrate its use for measuring lateral electric fields, it should also be possible to measure vertical electric fields with an additional vertical position modulation. The 2D electric field images demonstrated here are already an advance from lateral electric field line scans, and we envision applying the PM-KPFM technique to measure local electric fields in bulk heterojunction solar cell blends. The 2D electric field scans could show the current flow direction at domain boundaries near the open-circuit voltage $V_{oc}$.

References:
Fabrication of Semiconductor Nanostructured Thin Film Using Inkjet Printing

CNF Project Number: 1645-08
Principal Investigator: Tobias Hanrath
Users: Qiannan Wen, Eliad Peretz

Affiliations: School of Applied and Engineering Physics, Sibley School of Mechanical Engineering and Aerospace Engineering, Robert Frederick Smith School of Chemical and Biomolecular Engineering; Cornell University
Primary Source of Research Funding: National Science Foundation
Contact: th358@cornell.edu, qw97@cornell.edu, ep442@cornell.edu
Primary CNF Tools Used: Dimatix printer, Zeiss Supra SEM, ABM contact aligner, Heidelberg DWL2000, MVD 100

Abstract:
Semiconductor nanocrystals (NCs) have size dependent optical and electronic properties. The assembly of NCs building blocks into superlattice has opened up materials library by design. The fundamental processes governing the assembly and attachment of NCs into coherent artificial solids are not well understood due to the complexity of the system. Here we demonstrate the application of inkjet printing to form ordered lead sulfide NCs from sub-monolayer to multi-layer structures. The optimization of NCs/substrate interaction by surface functionalization, and the controlled liquid diffusion by confined area printing give insights into the nucleation and growth mechanisms of NCs superlattice. The printing technique shows the potential of decoupling reaction kinetics on small scale and advancing nano-patterning on flexible substrates in semiconductor microelectronics.

Summary of Research:
Semiconductor nanocrystals (SC NCs) have a size smaller than the bulk Bohr radius and quantum confined properties tuned by size, shape and surface chemistry. The self-organization of the NC building blocks forms connected-but-confined structure with their distinct electronic properties [1]. Among various thin film deposition methods, the printing technology is particularly interesting due to its compatibility with flexible electronics and large-scale device manufacture.

Minemawari, et al. [2,3], reported the formation of organic single crystal thin film using anti-solvent coupled inkjet printing and resolved the liquid contact dynamics triggering its crystallization. The NCs system however, is more complicated due to the multiple interaction pathways between the NCs core, ligand and solvent [4]. An understanding of the fundamental principle in NCs assembly and attachment is still lacking.

We demonstrated the fabrication of lead sulfide (PbS) NCs thin film using a Dimatix printer. A silicon wafer with a thin layer of oxide is deposited with a layer of S1818 and exposed to a mask with various pattern shapes (of dimension 100-1000 µm). The unmasked regions are coated with hydrophilic groups by UV-Ozone treatment. Another option is to grow monolayer of 3-mercaptopropyltrimethoxysilane (MPTMS) by molecular vapor deposition to increase the adhesion of nanoparticles to the substrate.

The Dimatix printer uses a disposable cartridge with 16 piezo-actuated nozzles controlled by a user-defined waveform. We dissolve the PbS NCs in dichlorobenzene. The ink is dispensed at 10 pL for each droplet at 2 m/s adjusted by the firing voltage. The printing protocol developed here is applicable to materials of the same class. Figure 1 is an illustration of the colloidal NCs inkjet printing on functionalized...
substrates. The inset presents the liquid jetting from cartridge nozzle and the hydrophilic/hydrophobic patterned substrate we use for printing.

The PbS NCs with size of 6 nm are assembled into hexagonal geometry with film thickness from submonolayer to multiple layers. Figure 2(a-d) show scanning electron microscopy (SEM) images taken on a dumbbell pattern deposited with PbS NCs. The variations in the film structures are correlated with the controlled liquid flow. In most regions of the pattern, the film forms monolayer to bilayer structures as shown in Figure 2(b). Inset is the Fourier transform showing hexagonal lattice. Figure 2(c-d) shows the sub-monolayer formation near the edge where solvent drying is initiated, and the multi-layer structures with array of holes at the center towards which liquid flow from the surroundings.

While the solvent evaporation driven assembly is a simple method for thin film deposition, the fast evaporation rate poses a major problem to the long range ordering of the NCs. Other limitations include difficulties in delivering chemical triggers for the superlattice transformation, in situ ligand exchange and multi-component assembly.

One of our ongoing research goals is to transfer the conventional liquid-air interface assembly in big troughs to the small scale experiments on a printer. Our preliminary test has been successful in depositing ethylene glycol as non-solvent on confined hydrophilic patterns, while the deposition of the NCs layer has more challenges regarding undesired mechanical perturbation and non-uniform spreading. Solving these problems will give further insights into the NCs assembly kinetics and promote the application of coherent NCs solid in semiconductor thin film technology. Our other investigations include the substrate functionalization that specifically address the surface chemistry of NCs during assembly and attachment, and different coating techniques applicable to large scale manufacture while preserving long range ordering of the NCs superlattice.

References:
**Microfabricated Germanium X-Ray Optics for the Cornell High Energy Synchrotron Source (CHESS)**

**CNF Project Number: 2172-12**

**Principal Investigators:** Arthur Woll\(^1\), Joel Brock\(^{1,3}\), Ernie Fontes\(^1\)

**User:** David Agyeman-Budu\(^2\)

**Affiliations:**
1. Cornell High Energy Synchrotron Source (CHESS), Cornell University;
2. Materials Science and Engineering, Cornell University;
3. Applied and Engineering Physics, Cornell University

**Primary Sources of Research Funding:** CHESS is supported by the NSF and NIH/NIGMS via NSF award DMR-1332208

**Contact:** aw30@cornell.edu, jdb20@cornell.edu, ef11@cornell.edu, da76@cornell.edu

**Website:** http://www.chess.cornell.edu/

**Primary CNF Tools Used:** Plasma-Therm Versaline® Deep Si Etcher

---

**Abstract:**

With microfabrication and deep reactive ion etching, we have developed an x-ray optic called the Collimating Channel Array (CCA) for confocal x-ray fluorescence (CXRF) using germanium substrates. This builds on our previous efforts where these optics were fabricated out of silicon and demonstrated to have a depth resolution of 1.7 µm. The etch mechanisms and comparison between Si and Ge substrates are highlighted.

---

**Summary of Research:**

Confocal x-ray fluorescence (CXRF) is a depth resolved x-ray microprobe technique used to spatially resolve the elemental and chemical speciation of thin films or virtual cross sections of materials that cannot be thinned. The technique is realized by isolating a probe volume formed by the overlap of the foci of a focusing optic and a collection optic. CCAs are excellent collection optics in this regard since its depth resolution is nearly energy independent and more flexible to design [1-5].

CCAs contain a set of radially arranged, collimating channels that point to a single source position at the focus. The channel geometry, which collects the fluorescent x-ray photons from the defined probe volume to the detector, is defined with staggered pillars. The range of energy where these optics are useful is limited by attenuation losses at higher energies with silicon substrates. Optics fabricated from germanium (Ge) substrates as an alternative can operate well up to 30 keV compared to 12 keV with silicon (Si).

Since there are very few publications on plasma etching of germanium and even fewer on deep etching, a study was done to compare the etch performance of Ge with Si. The etch chemistry of Ge to SF\(_6\) is similar and comparable to that of Si and as such, deep reactive ion etch recipes for Si also work well with germanium substrates. Using the Plasma-Therm Versaline® deep silicon etcher, a Taguchi L9 orthogonal partial factorial Design Of Experiment (DOE) was conducted to compared the trends of the etch rates by varying the ICP power of the three processing steps; polymer deposition, polymer removal etch, isotropic Si/Ge etch, and the peak-to-peak voltage of the polymer removal etch step.

The etch comparison done for 4 µm and 40 µm features shown in Figures 1 and 2 suggests that the etch mechanisms for Ge differ from Si and that accounts for the difference in the etch rates and trends of the Ge and Si. The Ge etch rate is higher for the larger 40 µm features and smaller for the 4 µm features when compared to the Si etch rates as shown in Figure 3.

There is a strong aspect ratio dependent etching (ARDE) effect with Ge compared to Si and this suggests that the Ge etch is more chemically dependent process and as such, more susceptible to RIE-LAG. This unusual etch response actually also makes Ge a preferred substrate for fabricating CCA optics as the optic design inherently imposes a variable loading effect. The desired larger features are preferred to etch as deep as possible while maintaining the structural integrity of smaller features to survive the etch.
2016-2017 Research Accomplishments

Process & Characterization

Figure 1: SEM profile of the etched 40 µm and 4 µm features in Si (A) and Ge (B).

Figure 2: Etch rate dependence on the Dep ICP power for the Si and Ge. The etch rate for the 40 µm features (A) is higher for Ge compared to Si but lower for the 4 µm features (B).

Figure 3: Comparison of ARDE with Ge (A) and Si (B) substrates demonstrating the differential etch rates for 4 µm and 40 µm trenches.

References:
Nanocale Periodic Features with DUV Stepper Backside Alignment

CNF Project Number: 2217-13
Principal Investigator: Ioannis Kymissis
User: Tanya Garza

Affiliation: Department of Electrical Engineering, Columbia University, New York, NY
Primary Source of Research Funding: National Science Foundation
Contact: johnkym@ee.columbia.edu, tcg2112@columbia.edu
Website: http://kymissis.columbia.edu
Primary CNF Tools Used: ASML 300C DUV, GCA 5x stepper, Oxford 100, P10 profilometer

Abstract:

Lithography with the ASML 300C DUV stepper has been used in previous years to produce pillar features with diameters including 232 nm, 306 nm, 408 nm, and 446 nm on the wafer frontside. This past year work with the ASML 300C DUV stepper was expanded to include backside features aligned to the frontside using the ASML 300C DUV backside alignment system. A process was developed where tool auto alignment could be done with backside alignment features etched into a fused silica wafer.

![Figure 1: SEM image of photonic crystal pattern, nominally with 270 nm pillar features, fabricated fused silica with process developed with ASML 300C DUV stepper.](image1.png)

![Figure 2: SEM image of photonic crystal pattern, nominally with 306 nm hole features, fabricated in fused silica with a process developed with ASML 300C DUV stepper.](image2.png)

Summary of Research:

In previous years, a process for patterning nanophotonic pillar and hole structures was developed at CNF that used the ASML 300C DUV stepper and the GCA 5x stepper. These features were etched into the substrate material using the patterned resist as an etch mask. The ASML 300C DUV stepper process has been used to pattern 4-inch borosilicate float glass wafers ("borofloat"), 4-inch fused silica wafers, and 4-inch silicon wafers. Pillar features like those shown in Figure 1 were fabricated with diameters of 232 nm, 270 nm, 306 nm, 408 nm, 612 nm and 816 nm. Hole features like those shown in Figure 2 were fabricated with design diameters of 306 nm, 408 nm, and 446 nm.

Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. Photonic crystal geometry was examined in the SEM and photonic crystal performance was assessed optically via extraction of waveguided light. Preliminary work was done with the GCA 5x stepper process to pattern 4-inch fused silica wafers for minimum hole feature sizes of 408 nm and 446 nm. The best results of a coarse DOF and exposure dose variation study on the GCA 5x stepper are shown in Figure 3.
This past year work was done to enable front and backside patterning of 4-inch fused silica wafers on the ASML 300C DUV stepper. Typically backside alignment is done in silicon with four ASML defined alignment patterns etched on four corners of the wafer backside. These ASML marks are diffraction gratings that reflect a laser light focused onto a sensor. These marks are etched to a target depth of 160 nm for bare silicon to optimize the signal strength on the sensor [1].

Two possible methods were considered to achieve backside alignment on fused silica. Since fused silica is highly transparent, processes where the ASML patterns in the material were coated with a thin 60 nm layer of aluminum were considered in addition to patterns in the bare fused silica. One minute of the oxide etch recipe on the Oxford 100 tool produced etched depths of 150 nm as measured by the P10 profilometer. With these etch conditions, alignment to three out of the four backside alignment marks was obtained. This level of alignment was found satisfactory. Repetition of this processes would sometimes yield alignment to only two out of the four backside alignment marks but this level of alignment was also considered satisfactory. Tests with aluminum over the alignment marks on fused silica have not yet been done.

Two ASML alignment marks were patterned on the wafer backside in addition to the four used for automated alignment on the DUV stepper. These additional alignment marks were used for contact lithography on the wafer backside in addition to the projection lithography done on the DUV stepper. Figure 4 shows an optical microscope image of contact alignment marks in resist overlaid on the ASML diffraction grating alignment marks etched into the wafer backside.

In summary, the process previously developed to pattern fused silica wafers with nanophotonic pillar and hole structures was expanded to include automated backside alignment on the ASML 300C DUV stepper. Work done to enable backside alignment was achieved for up to three out of four ASML alignment marks etched into bare fused silica to a depth of 150 nm.

References:
Efficient Template-Based Nano Manufacturing of Carbon Nanotube Arrays

CNF Project Number: 2334-15
Principal Investigator: Dr. Michael Schrlau
User: Devarsh Shah

Affiliation: Mechanical Engineering, Rochester Institute of Technology
Primary Source of Research Funding: NIH-R21 Grant
Contact: mgseme@rit.edu, dss1199@rit.edu
Primary CNF Tools Used: PT-740 etcher, Oxford 81 etcher

Abstract:
Carbon nanotube arrays have been found to be highly effective at carrying out the intracellular delivery of cargo at high efficiencies while ensuring cell viability. Template-based chemical vapor deposition is an efficient two-step process to synthesize carbon nanotubes (CNTs) for a wide range of applications. In this process, the choice of template dictates certain physical features of the carbon nanotubes (CNTs), such as length and outer diameter, while the process itself affects other features, such as tube wall thickness, carbon deposition rate, and carbon morphology. In this report, the manufacturing and fabrication process of carbon nanotube arrays is being described.

Summary of Research:
Carbon nanotubes (CNT) arrays are fabricated using commercially available anodized aluminum oxide (AAO) membranes. Anodized aluminum oxide (AAO) membranes are annealed in air at 730°C for 4 h and placed in a three-stage chemical vapor deposition (CVD) tube furnace. After purging the furnace with Argon, 30/70 (vol%/vol%) ethylene/helium precursor gas was flowed at 60 sccm into the furnace at 700°C for 5 h to deposit a thin film of carbon on all surfaces of the anodized aluminum oxide (AAO) membrane, including the walls of the membrane pores to form carbon nanotubes (CNTs) embedded in the anodized aluminum oxide (AAO) template.

The carbon layer on one side of the membrane was then removed using plasma etching (Oxford 81) at 300 mTorr, RF 250 W, and oxygen flow rate of 50 sccm for 45 sec. Carbon nanotubes (CNTs) were then partially exposed by selectively etching the anodized aluminum oxide (AAO) template using reactive ion etching (PT-740) with boron trichloride (BCl₃) at 15 mTorr, RF 500 W, and BCl₃ flow rate of 80 sccm for six hours.

The resultant carbon nanotube array as shown in Figure 2, with an average tip diameter of 205 ± 42 nm, tube wall thickness of 28 ± 5 nm, tube-to-tube spacing of 187 ± 36 nm protruding 176 ± 34 nm from the surface of the 13-mm diameter anodized aluminum oxide (AAO) membrane. Figure 3 shows the diagram of how the carbon nanotubes look after the first and second steps, for better understanding.

Dozens of carbon nanotubes (CNT) arrays devices were produced in a single manufacturing run and stored until needed for transfection.

References:
2016-2017 Research Accomplishments

Process & Characterization

Figure 1: SEM of carbon nanotubes (CNTs) array after the first step of processing.

Figure 2: SEM of carbon nanotubes (CNTs) array after the second step of processing.

Figure 3: Schematics of anodized aluminum oxide after the first and second step for better understanding.
1.1kV GaN Vertical Power P-N Diodes on Ammonothermal GaN Substrates; Process Development and Device Characteristics

CNF Project Number: 2350-15
Principal Investigators: Huili Grace Xing, Debdeep Jena
Users: Zongyang Hu, Wenshen Li, Mingda Zhu, Hank Liu

Affiliations: Electrical and Computer Engineering, Material Science Engineering; Cornell University
Primary Source of Research Funding: ARPA-E Sixpoint
Contact: grace.xing@cornell.edu, zh249@cornell.edu
Primary CNF Tools Used: Oxford PECVD, Autostep i-line stepper, PT770 etcher, SC4500 evaporator,

Abstract:
Vertical GaN power p-n diode processes have been developed using the CNF. The project includes device fabrication, imaging and electrical test of GaN homoepitaxial p-n junction structures on ammonothermal GaN substrates. High performance GaN-on-GaN vertical p-n diodes have been demonstrated. Large forward currents (forward turn-on voltage of 3.3V, forward current of 500 A/cm² at 4V and 1000 A/cm² at 4.5V), on-resistance of 0.72 mΩ∙cm² and reverse breakdown voltage of 1172V have been measured in these devices. Baliga figure-of-merit is calculated to be 1.9 GW/cm². This is the first demonstration of high voltage GaN p-n diodes on ammono GaN substrate.

Summary of Research:
Gallium nitride (GaN) has been widely considered as one of the most promising wide band gap semiconductors for development of next generation power semiconductor devices. The theoretical power performance of GaN predicted by the Baliga’s figure-of-merit is 1000x higher than that of Si and nearly 2x higher than SiC. Though record-high power diode performance has been demonstrated in GaN compared to all other semiconductor materials [1], the lack of low-cost, low-dislocation-density bulk substrate limits the feasibility of application for GaN based devices. The goal of the ARPA-E Sixpoint project is to develop high quality, inexpensive GaN substrates using ammonothermal method, and demonstrate high performance and repeatability of vertical GaN power devices. The development of fabrication processes for GaN based power devices is also acritical component in this project.

Device fabrication includes metal deposition (e-beam evaporation of Ti, Pd, Au), dry etching (Cl-based plasma etching), photolithography (Autostep i-line stepper), dielectric deposition (PECVD SiO₂), Device sizes are 50 µm ~ 700 µm. Optical microscope, profilometer and AFM are used frequently to observe sample surfaces during processes. The device processes and main CNF tools used are described briefly as the following:

1. Beveled p GaN mesa etching
   - SiO₂ mask deposition (Oxford PECVD)
   - Litho and wet etching of SiO₂ (Autostep i-line Stepper)
   - Dry etching of p GaN (PT770 etcher)
2. Top ohmic contact deposition
   - Litho and Pd/Au ohmic contacts (SC4500 evaporator)
3. Passivation
   - Dielectric passivation (Spinner)
   - Lithography
   - Wet etch to open contact holes
4. Field plate
   - Litho and field plate deposition, liftoff
5. Bottom contact deposition
   - Photoresist coating and cleaning
   - Ti/Au back ohmic contacts, liftoff

The schematic device structure is depicted in Figure 1. The epitaxial structure is grown by metalorganic chemical vapor deposition (MOCVD) on bulk GaN substrates. The thick (8 µm) n-GaN region is the most critical part for the electrical characteristics of the GaN p-n diodes. Compared to last year’s devices, the MOCVD growth condition in the most recent runs has been
tuned to control the charge concentration in the n-GaN layer within 2E15-1E16 cm⁻³ ranges. Other device parameters have been kept largely the same. The beveled mesa and field plates are designed to mitigate electrical field crowding at the edge of the p-n junction and the corners of the mesa [2].

An optical image of the GaN device chip after fabrication is shown in Figure 2. The devices have sizes ranging from 50 µm to 700 µm (the largest device is not shown in the figure).

The forward current-voltage curve of a typical GaN p-n diode is plotted in Figure 3. The forward current at V < 2.4V is lower than the lower limit of the measurement system (semi-log scale plot is not shown). The diode turns on at ~ 3.3V, and the current reaches 500 A/cm² at 4V and more than 1000 A/cm² at 4.5V, which meets our project goal for the forward current density. Devices with and without field plates do not show significant difference under forward biases.

The reverse current-voltage characteristics of a group of GaN p-n diodes with 110 µm diameter are plotted in Figure 4. The highest breakdown voltage measured is 1172V. The Baliga’s figure-of-merit (BFOM) is calculated to be 1.9 GW/cm², among the highest reported for GaN power p-n diodes. Capacitance-voltage measurement has been performed on these diodes, and charge distribution inside the n-GaN has been analyzed (results not shown due to limited space). The charge concentration ranges from 2 × 10¹⁵ cm⁻³ to 1 × 10¹⁶ cm⁻³ at different positions in the n-GaN. This is likely caused by gas flow fluctuation near edges of the 10 mm × 10 mm sample during the MOCVD growth, which leads to variations in impurity incorporation in the GaN layers.

Device mapping has been performed on the 10 mm × 10 mm GaN p-n diode sample. Breakdown voltages are measured between ~ 500V to ~ 1000V on different devices with the same size (110 µm diameter). It has been found that the surface roughness (instead of charge concentration in the n-GaN) is likely the main factor that leads to the non-uniform breakdown voltages.

Future work from Sixpoint will be growths on 2-inch ammono GaN substrates to demonstrate high breakdown voltage p-n diodes with good uniformity across the wafer.

References:

Figure 1: Schematic cross section of a vertical GaN power p-n diode with field plate edge termination. Figure 2: Part of a GaN power p-n diode chip imaged under the optical microscope. Figure 3: Forward current-voltage characteristics of a vertical GaN power p-n diode. Figure 4: Reverse current-voltage characteristics of a vertical GaN power p-n diode with a breakdown voltage of 1172V.
Deep-Tissue Photonic Needles

CNF Project Number: 2364-15
Principal Investigator: Michal Lipson
User: Romy Fain

Affiliations: Electrical and Computer Engineering, Cornell University; Electrical Engineering, Columbia University
Primary Source of Research Funding: National Science Foundation
Contact: ML3745@columbia.edu, rmf98@cornell.edu
Primary CNF Tools Used: Woollam spectroscopic ellipsometer, ABM and SÜSS MA6-BA6 contact aligners, ASML 300C DUV stepper, Heidelberg DWL2000, Zeiss Supra and Ultra SEMs, CSI PECVD, Oxford ALD and PECVD

Abstract:
We demonstrate a new platform for minimally invasive, light delivery probes leveraging the maturing field of silicon photonics, enabling massively parallel fabrication of photonic structures. These photonic needles probes have sub-10.µm cross-sectional dimensions, lengths greater than 3 mm — surpassing 1000 to 1 aspect ratio, and are released completely into air without a substrate below. We show the photonic needles to be mechanically robust when inserted into 2% agarose. The propagation loss of these waveguides is low — on the order of 4dB/cm.

Summary of Research:
The use of light for biological imaging and stimulation, in the near and far field, has an array of useful applications, but due to combined scattering and absorption effects in tissue, current techniques require significant damage to the tissue when reaching past a couple of millimeters into deep tissue.

Ground-breaking early light delivery probe schemes have included large chip shank-like designs [1-3] reminiscent of traditional electrode on chip platforms [4,5] fiber-like devices [6,7] or designs with traits of both [8,9]. When these schemes reach deep tissue they have large cross-sections on the order of 100 µm across or more. They are destructive to the biological tissue, inducing an immunological response, disrupting the system we want to measure, but also impeding the signal response collected [10-12]. Our approach is to provide high aspect ratio Photonic Needles long enough to reach deep-tissue, but narrow enough to provoke minimal immune response.

High quality photonic signals can be guided in nano-waveguides as small as a few hundreds of nanometers in cross-section, but how small of a cross-section can we make before buckling occurs and a deep tissue probe fails, either mechanically or optically?

We have demonstrated:
• 1000:1 aspect ratio
• 3.5 mm long released, no substrate
• Concurrent mechanical and optical robustness
• Minimum cross-section 3 µm wide, up to 3.5 mm long
• Mechanical stability down to 3µm x 10µm x 3.25mm long
• Array of 18 photonic needles
• Low loss: 4 dB/cm average

Ultra long and narrow photonic needles could enable longer-term chronic studies and insertion of very large arrays of needles by:
• Displacing only a negligible volume of tissue
• Providing stronger signals and more accurate data
• Allowing the stimulation and imaging of individual neurons across large volume cell circuits in real time
Figure 2: Optical loss testing results. This graph shows the measured propagation losses in waveguides with dimensions that survived mechanical testing without buckling using the Fabry-Perot cavity between the input and output facets.

Figure 3: The mechanical testing of Photonic Needles. Images (left) are of a 3 × 10 µm cross-section probe approximately 3.25 mm long, with a.) microscope image of it being inserted into 0.5% agarose, and b.) angled SEM of tip. c.) Composite microscope image demonstrates a full double set of released probes being inserted into 2% agarose, to simulate mouse cortex with dura [24,25]. Buckling needles are colorized in [red].

Figure 4: Buckling results for Photonic Needles. This graph describes the mechanical testing results from the insertion of a full chip array of Photonic Needles into 2% agarose (see also photo Figure 2c.), as compared with applied theory. Angled and radiused tips have an estimated 30% and 50% tip area respectively, compared to a blunt tip surface area (see also SEMs in Figure 1c). Blunt tip critical force [20] is scaled for decreased cross-sectional tip area. Theoretical shaded areas are bounded by Euler buckling theory for fixed/fixed above and fixed/pinned below.

References:
Abstract:

This project centers on the incorporation of multilayer graphene with ultrathin polymer support as x-ray transparent vacuum-tight window material. Possible applications include microcrystallography and biological small angle x-ray scattering (bioSAXS) flow cells for use in diffraction studies at the Macromolecular Diffraction Facility at the Cornell High Energy Synchrotron Source (MacCHESS). Graphene is a 2D hexagonal carbon lattice that has remarkable electrical and mechanical properties. Due to extraordinary tensile strength graphene has shown much promise as being able to hold vacuum at a thickness of just a few atoms [1]. This is important because reduction of material within the x-ray beam path can reduce the background scatter that is highly problematic in microcrystallography and bioSAXS.

Summary of Research:

The goal of this work was to explore the fabrication of graphene-based vacuum-tight windows for x-ray specimen cells. The areas that need to be covered span tenths of a millimeter, thereby necessitating multilayer graphene. The need for > 20-25 layers of graphene to achieve the goals of this project led to several different methods for obtaining multilayers of graphene. During the initial stages of this project, mono-bi-trilayer graphene was used for manual assembly of layers [2]. The process of manual layer assembly is both time intensive and highly delicate, with a low yield of intact and useable graphene-based pieces. One of the solutions to this problem is to grow large grain multi-layer graphene (LGMLG) that is strong enough to stand alone with no polymer backing, see Figure 1. The LGMLG covering the 150 µm diameter windows remained intact through diffraction data collection.

This was accomplished by adapting a chemical vapor deposition (CVD) process using the First Nano Carbon Nanotube and Graphene (CNT/Graphene) Furnace with the help of Phil Infante. We combined several graphene recipes to optimize the characteristics of LGMLG. The initial multilayer graphene recipe could produce greater than tetra-layer graphene on copper by increasing the pressure within the growth chamber during the growth step [3]. This was accomplished by increasing the hydrogen gas flow to the maximum rate while also reducing the power of the vacuum pump. Analysis with Raman spectroscopy showed that graphene growths done at 240 mTorr produced non-uniform layers that were sometimes bilayer and often greater than four layers of graphene. These results were confirmed through scanning electron microscopy (SEM), using the Zeiss Ultra high-resolution field emission SEM at CNF.
Since graphene is weakest at the grain boundaries [1], and the size of the windows exceeded the size of the grains we were producing, we attempted to increase grain size in hopes of growing larger grains. Introducing an oxidation step before the growth step has been shown to increase grain size and thus reduce the occurrence of boundaries over large monolayer growths [4]. Our recipe combined the multilayer inducing pressure increase, with an oxidation step to produce LGMLG.

In Figure 2, A/B is multilayer growth without an oxidation step, and C/D is after optimization of the oxidation step. This comparison shows that the irregularities in grain size were reduced and that overall grain size was increased. However, it was not a significant enough increase and the LGMLG was not able to hold vacuum. We then tried growing LGMLG with a thin PMMA polymer backing layer, under the rationale that the graphene would serve as a layer that was gas and water vapor impermeable and the PMMA would add sufficient strength to hold the vacuum. The graphene-PMMA material was indeed vacuum tight, but when tested for x-ray scatter it was realized that the material had significant SAXS, possibly due to carbon particles produced during the synthesis. Figure 3 shows the SAXS from kapton, glass, and graphene-PMMA windows. It is observed that commercially available Kapton® and glass windows have lower SAXS backgrounds than the graphene-PMMA windows.

Conclusions:
We failed to produce a graphene-based x-ray window that was both strong enough to withstand vacuum over a 150 µm diameter aperture and yet had a lower SAXS background than commercially available alternative window materials. Further work is required to make better multilayer graphene sheets that do not require a polymer support.

References: