Hydrophobic/Hydrophilic Nanoscale Patterns for Enhanced Pool Boiling

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Abstract:

Raising pool boiling capacity via increase of critical heat flux is critical to emerging technology as ever-higher heat flux is demanded for operation. Power generation systems are stretching the limits of boiler output and more rapid cooling is needed to accommodate the newest generation of electronic devices. Researchers are seeking critical heat flux enhancement on modified surfaces which are durable and capable of being scaled up to industrial application. Critical heat flux enhancement has been attained by increasing surface wickability, adding surface roughness, creating thermal gradients, and introduction of capillary pumping effects. In this work, surfaces with nanoscale hydrophobic/hydrophilic patterns were created using current nanofabrication techniques to pattern hydrophobic silane onto a silicon dioxide surface. Improvement in critical heat flux was achieved by evaporation of the microlayer, which resulted in an elevated bubble growth rate that caused a delay in the onset of dry out. The highest performance observed in this study was a surface capable of evaporating off ~ 300 nm of microlayer height early, yielding a critical heat flux of 124.4 ± 1.5 W/cm², a 53% enhancement. These surfaces demonstrated pool boiling enhancement with no increase in surface area, capillary pumping effects, thermal gradients, additional roughness, nor complex/fragile nanostructures.

Summary of Research:

Boiling is a widely used heat transfer process in industrial power generation and commercial applications since it is a simple method to transfer large amounts of thermal energy. In pool boiling, the primary mechanism of heat transfer is the nucleation and growth of vapor bubbles on the heated surface. As these bubbles grow and detach, latent heat is imparted to the stationary fluid. Because heat flux through the surface is proportional to the rate of nucleation and vapor expansion, this flux is capped at the limit when bubbles do not depart quickly enough and coalesce into a film on the surface. This film, referred to as “dry out,” insulates the fluid from the heating surface, causing a rapid drop in heat flux and in surface temperature. Critical heat flux is the maximum rate of heat transfer achieved before the dry out phenomenon occurs; industrial boilers must operate well below CHF as the temperature spike would damage the surface.

Manipulation of the boiling surface to raise CHF and improve the heat transfer coefficient (HTC), or rate of heat transfer per unit superheat (temperature difference between the surface and fluid), is necessary to meet the demand for increasing heat flux in power generators and electronics [1].

For this study, surfaces targeting CHF enhancement were fabricated using standard nanofabrication techniques on silicon wafers. The surfaces were comprised of a base layer of hydrophilic silicon dioxide (SiO₂) with nanoscale patterns of a hydrophobic silane. This resulted in variation of wettability across the surface. In order to test these samples in pool boiling experiments, a 500 nm film of copper was deposited on the back of the sample to be soldered to a copper heating rod in the boiling chamber.

Samples were fabricated at Cornell NanoScale Science and Technology Facility (CNF), a National Nanotechnology Infrastructure Network site. All materials and supplies were purchased from the cleanroom at CNF. The nanoscale patterns were fabricated onto the
front side of silicon wafers and a layer of copper (Cu) was deposited on the backside for coupling with a heater (Figure 1). Standard 100 mm N/Ph silicon wafers were cleaned per the semiconductor industry standard RCA clean, which is comprised of acid and base dips.

The wafers were first dipped for 10 minutes in a base bath of ammonium hydroxide and hydrogen peroxide held at 70°C. After rinse in deionized (DI) water, wafers were dipped in a bath of hydrochloric acid and hydrogen peroxide to remove metallic impurities. The wafers were then processed in a wet/dry oxide furnace to grow a uniform, 125 nm thick layer of SiO2 on both front and back surfaces of the wafer. Oxide was grown in wet conditions (with the addition of steam to the furnace) at 900°C for 54 minutes. Immediately before Cu was deposited on the backside of the wafers, both front and back were cleaned under oxygen plasma for 60 s in an Aura 1000. A 10 nm adhesion layer of titanium (Ti) was deposited to provide strong adhesion between SiO2 and Cu. A 500 nm film of Cu was subsequently evaporated onto the substrate.

The evaporation chamber was initially pumped down to $2.0 \times 10^{-6}$ Torr and vacuum was held through both Ti and Cu evaporation. The nanoscale patterns were then transferred to the front side SiO2 surface via photolithography (Figure 1). An anti-reflective coating (ARC) was spin-coated onto the surface before photoresist deposition to improve exposure accuracy. DSK 101-312, a developer soluble ARC, was used for compatibility with the lift-off procedure and stability of silane. A 500 nm thick layer of negative photoresist (UVN 2300) was spun over the ARC and baked.

The pattern was transferred to the resist by deep ultraviolet (DUV) exposure in an ASML 300C DUV Stepper at an exposure intensity of 17 mJ/cm² and 0 µm focus; these parameters were determined by scanning electron microscope (Zeiss Ultra SEM) analysis for precision to the desired pattern dimensions. After development, silane was deposited in an MVD 100 molecular vapor deposition chamber for 10 minutes of reaction time. The lift-off procedure was completed by stripping the photoresist in an acetone bath and developing off the ARC, yielding a SiO2 surface patterned with silane (Figure 2).

References: