Electrical Characterization of Si+ Implanted InGaAs under Laser Spike Annealing Using Micro-Van der Pauw Devices

CNF Project Number: 150-82
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Abstract:
The sub-ms annealing times of laser spike annealing (LSA) have the potential to increase activation of Si implants in In_{0.53}Ga_{0.47}As (InGaAs) to levels necessary for use in future generations of CMOS technology. The high temperatures and short times of LSA allow for metastable activation and extended process temperatures. Single stripe LSA scans were conducted to probe the activation as a function of annealing temperature. Micro-Van der Pauw devices were fabricated in 5 µm steps in order to directly measure sheet resistance and carrier concentration across a single laser stripe, thus providing the full behavior as a function of temperature. These measurements are correlated with non-invasive Raman measurements of carrier densities which indicate activation in a narrow temperature range between 800°C and 850°C. These measurements are crucial to establish conditions for future studies of Si activation by LSA.

Background:
Challenges lie ahead as silicon (Si) transistor technology enters the sub-10 nm regime. Ultimately a shift towards a brand new technology is needed (such as spintronics), but a possible solution to continue scaling over the next few decades is to replace silicon as the conductive channel material with higher mobility materials. In_{0.53}Ga_{0.47}As (InGaAs) is a strong candidate for low power n-channel complementary metal oxide semiconductor (CMOS) devices due to its high electron mobility of up to 10^5 cm^2V^{-1}s^{-1}. However, challenges arise when attempting to maximize dopant activation during thermal processing.

In this project, the potential of sub-millisecond LSA to improve the activation of Si+ dopants in InGaAs was explored. LSA uses a continuous-wave, line focused laser to rapidly anneal materials. The rapid quench of LSA is likely to prevent As loss to higher temperatures than other annealing techniques. Thus metastable annealing could allow for higher activation levels and potentially a reduced impact from the amphoteric effect. For research purposes, performing tests across a single laser stripe is extremely powerful as it allows for testing over a range of temperatures within a small area.

Summary of Research:
All measurements were performed on 6×6 mm samples of 10^{14} dose at 20 keV Si implanted InGaAs on InP substrates. Samples were laser annealed and subsequently patterned for direct mobility measurements using Micro-Van der Pauw structures (VDP). In order to perform Hall measurements across a single 600 µm wide laser stripe, extremely small VDP devices are necessary. Given typical lateral temperature gradients on the order of 5 K/µm, VDP probe areas were required to be on the order of 5 µm to achieve less than 25 K variation across the devices. Fabricating such small devices on annealed InGaAs was challenging due to poor metal adhesion and surface impurities. Indeed, multiple iterations of the process were necessary.
The VDPs were designed to be 5×5 µm squares with metal contacts. To etch trenches down to the InP layers in order to isolate the InGaAs VDPs, the samples were etched for 4 min in Ar/BCl3/Cl2 at an RIE RF power of 100 W and pressure of 5 mTorr. A standard lift-off process was initially used to create Ti/Au/Ni contact pads; however strain in the thick film caused delamination. Additionally, the lift-off process inconsistently removed the metal layer, likely due to impurities on the InGaAs surface inhibiting the photo resist removal. To avoid these issues, a wet etch process was developed to create the Cr/Au contact pads as seen in Figure 1.

Sheet resistances were measured initially in order to determine the feasibility of these devices. Using two point measurements, low ohmic contact resistances were achieved for all samples. A four point probe configuration was then used to measure sheet resistance in four directions. The sheet resistance ($R_s$) for each sample was calculated using the Van der Pauw method [1].

<table>
<thead>
<tr>
<th>Sample</th>
<th>Annealing Condition</th>
<th>Sheet resistance ($R_s$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InGaAs: p-type InP</td>
<td>CO$_2$ 250 µs 40 Watts (~500 °C)</td>
<td>29 ± 8</td>
</tr>
<tr>
<td></td>
<td>CO$_2$ 500 µs 37.5 Watts (~500 °C)</td>
<td>31 ± 6</td>
</tr>
</tbody>
</table>

Figure 2: Sheet resistance data from InGaAs VDPs.

Annealing temperatures and sheet resistances are outlined in Figure 2. Figure 3 shows an example IV curve for the VDP sheet resistance measurements under CO$_2$ laser anneal. The sheet resistance is linear and symmetric for all four possible configurations. Similar behavior and values are seen across all 16 devices tested at each annealing condition. While the VDP device data is clean and reproducible, the implied sheet resistance values are about four times smaller than the lowest possible sheet resistances for this annealing temperature.

In the absence of any experimental issues with the measurements, the validity of assumptions underlying the VDP technique were examined. Chwang, et al., experimentally and theoretically determined a correction value for non-ideal contacts on VDP samples [2]. The actual sheet resistance can be determined by multiplying the measured sheet resistance by a correction factor as seen in Figure 4. For the device design used, the ratio δ/l far exceeds the maximum ratio of 0.25 tested or calculated in Reference 2.

In the future, a new design will be necessary to create devices that better fit the Van der Pauw method criteria. If 5 µm$^2$ VDPs are desired, it is necessary to create contacts with lengths less than 1.25 µm to accurately use this correction factor determined by Chwang, et al. [2]. Given that the contact resolution limit is 2 µm, these contacts will not be possible using the current process. It will be necessary to switch to projection lithography with a resolution limit below 0.5 µm. Obtaining a consistent process that can accurately and directly measure the sheet resistance, mobility, and carrier concentration is necessary for future studies of InGaAs under Laser Spike Annealing.

References:
Transport Characterization of Monolayer and Bilayer Transferred Epitaxial (0001) SiC Graphene

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Abstract:
Silicon carbide (SiC) epitaxial graphene holds promise of high quality large area graphene sheets that are suitable for the manufacture of high mobility devices. We investigated the quality of monolayer and bilayer transferred epitaxial graphene of the Si-face SiC. Transport measurements were conducted using backgate method. Emphasis was on the mobility and doping levels that can be extracted from the devices and how they’re affected by annealing and other processes.

Figure 1: [A] AFM images of epitaxial graphene before transfer. [B] FETs and TLMs used for measurements.

Summary of Research:
Monolayer graphene was grown on the silicon face (0001) of silicon carbide (SiC) by sublimating the silicon atoms. The growth is carried out at near atmospheric pressure with a flow of argon at temperatures ranging around 160°C. This produces uniform monolayer graphene with excellent surface topology as described in Reference 1. The monolayer graphene is partially covalently bonded to the SiC substrate via what is called the buffer layer, which is a carbon rich reconstruction of SiC [2]. This buffer layer is electrically inactive. However, it does greatly degrade the mobility of graphene due to carrier doping and scattering [3]. This makes it difficult to properly characterize SiC graphene because its true physical properties are skewed by the SiC substrate effects. Characterization methods such as TEM also prove to be difficult for epitaxial graphene because of the difficulty of etching SiC.

The weak covalent bonding between epitaxial graphene and the SiC substrate has proven a challenge for transferring graphene. We have successfully transferred epitaxial graphene off (0001) SiC that is grown using the more recent atmospheric pressure growth. Initial characterizations using Raman show the clear sign of a monolayer graphene. The Raman sign of monolayer graphene is greatly enhanced and clearly distinctive once the graphene was transferred off the SiC substrate and onto SiO2. The graphene was also transferred onto a TEM grid by a collaborating group where TEM images were acquired clearly showing monolayer graphene [4]. Furthermore, the intercalation method [5] was used along with varied growth condition to further control and characterize more than monolayer graphene. Currently bilayers are being investigated with Raman and TEM.

Hall bars, field effect transistors (FETs), and transmission line measurements (TLMs) have been fabricated in an effort to characterize the mobility of these transferred epitaxial graphene as well as reduce contact resistance. Mobilities ranging around 1800 (cm²/V.s) were consistently measured for the monolayers and around 200 (cm²/V.s) for the bilayers. Carrier concentrations were measured in the range of 5 x 10¹⁰ (cm⁻²) for monolayers and in the
range of $1 \times 10^{13}$ $(cm^{-2})$ for the bilayers. When the bilayer graphene devices were annealed in an argon atmosphere at 300°C, the carrier concentration dropped to the range of $5 \times 10^{12}$ $(cm^{-2})$.

Graphene is transferred off SiC and onto silicon substrates, which have been oxidized using the CNF oxidation furnaces. Typically an oxide thickness of 100 nm is used. Standard photolithography using the ABM contact aligner or the 5X proximity aligner are used for both forming the graphene and depositing Ti/Pd contacts of thickness (0.5nm/150nm) respectively. The YES asher or the Oxford RIE dry etch are used for graphene forming. Electrical measurements are being carried out at room temperature at the CNF IV probe station. The graphene furnace was used for annealing purposes.

References:


Figure 2: [A] Mobility vs. carrier concentration for monolayer graphene. [B] Bilayer devices with backgate showing the dirac point before and after annealing.

Figure 3: [A] Raman spectra of epitaxial graphene after transfer. Notice the considerable increase in Raman counts. [B] Raman spectra of bilayer graphene.

Figure 4: TEMs of transferred monolayer epitaxial graphene [4].
Accurately Measuring Local Electric Fields
Using Kelvin Probe Force Microscope

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Abstract:

We have fabricated bottom-gate, bottom-contact transistors, which were used to demonstrate a new frequency-modulated Kelvin probe force microscopy (FM-KPFM) technique that directly measures local electric fields over semiconductor devices. We have also electrochemically grown poly(3,4-ethylenedioxythiophene) perchlorate films of varying work functions on one electrode of transistor substrates, which will allow us to study how charge injection and local electric fields depend on electrode work function with our new FM-KPFM technique.

Summary of Research:

Organic semiconductors are promising transistor and solar cell materials; however, charge transport and charge separation in these materials are still not well understood. Competing charge transport theories for organic semiconductors predict different relationships between charge mobility, electric field and charge density. Accurate microscopic measurements of electric fields can help evaluate contact resistance when the potential drop at the electrode is small, differentiate between charge injection mechanisms, and enable microscopic mapping of mobility across an operating transistor channel. Typically, local electric fields are obtained by taking the derivative of local surface potentials measurements obtained from Kelvin probe force microscopy experiments. Since derivatives act as high-pass filters, this numeric differentiation introduces noise into the electric field measurement.

We have invented a variation of frequency-modulated Kelvin probe force microscopy (FM-KPFM) that directly measures local electric fields by introducing an oscillating component into the stage scanning motion (Figure 1). By tracking the surface potential continuously in time, we can measure the amplitude of the surface potential oscillations, which are directly related to the electric field. We are essentially using position modulation to take the spatial derivative of potential, instead of calculating a numeric derivative.

We deposited a thin film of a perylene diimide (PDIF-CN2) onto transistor substrates fabricated in CNF. We measured the surface potential across these transistor channels using our new position modulation experiment.
at various drain and gate biases. A sample of the raw data is shown in Figure 2. We obtain much greater signal-to-noise ratios using our direct electric field measurement than by numeric differentiation, as shown in Figure 3, where the numerical derivative \( \frac{dV}{dx} \) is overlaid with the direct measurement (PM). We anticipate that this method will be especially useful for measuring small local electric fields in photovoltaic devices.

Immobile, background charge carriers are often neglected in the study of organic solar cells, but may play an important role in limiting solar cell power conversion efficiency. Over organic bulk heterojunction solar cell donor-acceptor blends, the surface potential varies dramatically based on the background charge carrier density, as revealed by KPFM measurements [1,2]. This background carrier density is determined by the work function of the underlying electrode, which is usually modified by a thin hole conducting / electron blocking layer, such as poly(3,4-ethylenedioxythiophene) (PEDOT).

In order to study the effect of background carriers, we have systematically varied the workfunction of poly(3,4-ethylenedioxythiophene) perchlorate (PEDOT:ClO\(_4\)) films electrochemically deposited on bottom contact, bottom gate transistors [3]. An atomic force microscope image of a deposited PEDOT film is shown in Figure 4. By growing PEDOT films with different workfunctions on the transistor source and drain electrodes, we will be able to directly see the effect of electrode workfunction and background charge density on charge injection or separation and local electric fields using our new FM-KPFM technique.

References:
Nanoscale Periodic Features Using DUV Lithography

CNF Project Number: 2217-13
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Abstract:
Deep ultraviolet (DUV) lithography has been investigated as a faster alternative to electron beam lithography for patterning nanophotonic structures including photonic crystals. This past year, previous investigations were expanded to include optimization for DUV42P antireflective coating in lieu of AR3, investigation of holes in lieu of pillar geometry, investigations of slightly larger minimum feature diameters of 270 nm, and investigation of dicing effects on die sidewall geometry for the purpose of wave-guiding light into the photonic crystal patterns.

Summary of Research:
Last year, a process for patterning nanophotonic structures was developed at CNF that used DUV projection lithography to pattern 4-inch borosilicate float glass wafers (“borofloat”), 4-inch fused silica wafers, and 4-inch silicon wafers [1]. Pillar features in a pit — like those shown in Figures 1 and 2 — with diameters of 232 nm, 306 nm, 408 nm, 612 nm and 816 nm were patterned using UV210-0.3 resist with AR3 antireflective coating, exposed with the ASML DUV lithography system, and was then etched with the Oxford plasma etchers. Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica wafers by varying these parameters incrementally and examining the resultant features.

Photonic crystal geometry was examined in the SEM and photonic crystal performance was determined by examining the optical context of extraction of wave-guided light.

The process developed previously using AR3 anti-reflective coating was re-optimized about the previous optimal conditions using DUV42P anti-reflective coating. Optimization was done for pillar features with diameters of 232 nm and 306 nm etched into fused silica. DOF, exposure dose, and etch depth were varied incrementally and examined to determine the exposure parameters which produced optimal geometry uniformity when inspected with the SEM and which gave the highest throughput when examining the extraction of wave-guided light. During this optimization process the higher throughput was found for parameters far from the previous optimal point. These features were highly distorted and looked more like holes than pillars when examined in the SEM. Neglecting these highly distorted patterns gave optimal exposure parameters and etch time close to that which was determined for the AR3 process. The latter optimal process parameters were considered to be best since they gave the least distorted geometry with the highest throughput.
Given that the results of the optimization showed distorted pillar patterns that looked more like holes than pillars gave higher throughput, hole patterns were investigated with a new commercially made mask. The exposure and etch parameters that were determined to be optimal from the pillar optimization were used in a first attempt to make these features which gave way to the features shown in Figure 3. It appears that the exposure conditions did not lead to complete development of the hole areas, which caused uneven etch depths during etching. Further work with holes will entail higher exposure doses and variations in the DOF parameters to see if that gives more complete development of the hole features.

It was previously found that the smallest of the features made that had a diameter of 232 nm developed a diamond shape even though the mask feature was an octagon and these small features also had a webbing effect between the pillars, clearly seen in Figure 1. It was believed that this feature distortion and webbing was due to the lower resolution limits of the ASML DUV stepper tool and so slightly larger 270 nm diameter features were added the new commercially made mask to see if this would improve resultant feature resolution [2]. The slight increase in feature size eliminated webbing effects seen between the pillars as can be seen in Figure 2. This increase in feature size did not result in octagonal features in lieu of diamonds however previous work has shown that features with a diameter of 408 nm or larger will be octagonal.

Diced die-edge quality effects how much light can be butt-coupled into the substrate containing the nanophotonic pattern. It was initially seen that dicing to the maximum depth allowed resulted in an edge with a small bit of glass footing at the bottom of the cut. In an attempt to remedy this problem, thicker dicing tape was purchased. Dicing tests were conducted with 268 µm thick tape and dicing depths ranging between 75 to 275 µm in 25 µm increments where depth is measured as the uncut portion of tape. These tests intended to determine which cutting depth resulted in the least amount of chipping without leaving footing on the die. It was found that more shallow cuts led to less chipping but cuts more shallow than 225 µm resulted in footing that can be seen in Figure 4. Thus an optimal depth of 225 µm was determined resulting in 43 µm blade depth into the tape.

In summary, the DUV process described previously has been further developed to include an optimized process with an alternative anti-reflective coating and preliminary work on hole features in addition to pillars has been done. The resolution limits of the process was also further refined to show that webbing seen in 232 nm diameter features is eliminated for diameters of 270 nm and higher. Work was done to determine an optimal dicing depth of 43 µm into dicing tape to eliminate footing on the bottom of the die edges with minimal chipping.

References:
Ion Milling of Mica

CNF Project Number: 2320-14
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Abstract:

The AJA ion mill at CNF was used to etch patterns in mica sheets. Etch rates were measured as a function of the ion beam voltage (and current) and angle of incidence.

Summary of Research:

A brief project was conducted to determine if the AJA ion mill could be used to etch features in insulating mica sheets. The beam voltage (and current) and ion beam angle were varied to determine their effect on the etch rate.

The AJA ion mill at CNF has a 22-cm diameter Kaufman and Robinson RF ion source and a 15-cm diameter (6-inch) rotating/tilting water-cooled substrate stage shown in Figure 1. Argon is the working gas operating at \( \sim 2 \times 10^{-4} \) Torr. Users can select any of the four ion beam operating conditions that have been programmed by the CNF tool manager. We used the two lowest voltages (See Table 1).

Mica sheets were mounted with wax to 2-inch diameter silicon wafers for handling and then patterned by photolithography for ion milling. Each wafer was attached to the ion miller carrier with two metal clips. Thermal transfer grease was not used. One wafer was used for each test, except two wafers were mounted as shown in Figure 2 for an additional test to check etch rate uniformity. The carrier mounts with a center screw to the substrate stage (chuck) in the ion miller.

Etch times varied from 3 to 8 minutes. There was no evidence of photoresist burning, and the resist was easily removed with acetone.

Figure 3 shows the etch rate vs. beam current and voltage at a 55-degree beam angle (beam angle = 90° - stage angle). The etch rate scales almost linearly with ion beam current, but not voltage. The etch rate was within ± 2% for multiple points on each wafer. The run-to-run etch rate was consistent to within ± 5%, but the ion source power supply became unstable at 400 volts (later corrected by CNF staff), so we increased the beam to 600 volts for our remaining experiments.

Figure 4 shows the etch rate vs. beam angle from 45 to 65° at 600 volts with points at 55°, 400 volts for reference.

<table>
<thead>
<tr>
<th>Program</th>
<th>Voltage [V]</th>
<th>Current [mA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>400</td>
<td>133</td>
</tr>
<tr>
<td>2</td>
<td>600</td>
<td>289</td>
</tr>
<tr>
<td>3</td>
<td>800</td>
<td>449</td>
</tr>
<tr>
<td>4</td>
<td>1000</td>
<td>627</td>
</tr>
</tbody>
</table>

Table 1: Pre-set voltages and currents for the RF ion source.
Figure 1: Wafer on rotating, tilting chuck in ion milling chamber.

Figure 2: Two-inch mica sheets on silicon wafers on the substrate carrier.

Figure 3: Etch rate vs. beam current and voltage at 55 degree beam angle.

Figure 4: Etch rate vs. beam angle at 600 volts, 289 mA.