A Single Lithography Self-Aligned Vertical NanoRelay

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Abstract:
We demonstrate the use of torsion in nanorelays to achieve low voltages, high speeds, single lithography step construction, and a form useful for configurability and electronic design enhancements in three-dimensional integrated implementations. The combined bending and torsion of self-aligned nanopillars facilitates the first top-down fabricated vertical three terminal nanoscale relay. Experimental devices, even at 500 nm features, operate at \( \sim 10 \) V and \( \mu \)s. Scaling suggests operation down to unit volts.

Introduction:
Nanorelays are potentially relevant devices for low standby power and energy exchanging computing [1] and for dynamic or non-volatile configurability. To date, nanorelay implementations have used processes that combine single crystal materials and layered structures, thus permitting ultra-small gaps needed for actuation. This allows electronics compatible voltages to be achieved at the expense of complex processes with high temperature deposition and selective removals.

Although recent planar structures based on CMOS-compatible top-down approaches have exhibited promising switching behavior [2, 3], they require either more real-estate or more aggressive scaling to achieve the high-aspect ratios necessary for low voltage operation. Vertical switches employing growth approaches based on nanotubes [4] have also been successfully demonstrated at low voltages with small device footprint. However, they require elaborate fabrication processes, use exotic materials and suffer from substantial variability in placement and size. We show here an appealing alternative, leveraging torsion, that has the potential to alleviate the need of single crystal deposition processes, and that can also be used in interposers for 3D integrated programmability. Using a single step of optical lithography, the device combines the benefits of a top down approach with the area savings of a vertical structure to achieve self-aligned nanopillars with aspect ratios up to 100:1.

Design:
Figure 1(a) shows vertical device which uses a combination of bending and torsion to physically connect S and D electrodes via a “channel.” With S/D grounded, \( C_{SC} \) and \( C_{DC} \) are in parallel with \( C_{BC} \) for a total equivalent capacitance \( C_{PC} \). Therefore, the gate to “channel” capacitance \( C_{GC} \) in series with \( C_{PC} \) form a voltage divider which determines the potential of \( C \), and the electrostatic force on the channel is proportional to \( V_{GC}^2 \). Electrostatic actuation of the “channel” results primarily in bending of the pillar until pull-in occurs.
Torsion allows self-correction for S/D offsets arising from line edge roughness or metal grain size. This is critical to achieving reproducible contacts in small geometries, an issue with conventional nanorelays.

Initial pull-in converts the device to a simple parallel plate configuration (Figure 1(d)) with new gap size determined by a predefined offset between a recessed gate and S/D, ~ 100 nm for current device. The recessed gate prevents gate–channel contact. This “new” gap is much smaller, thereby strongly enhancing torque on the channel. The device achieves an “ON” state when torsion overcomes the small S/D offset, establishing a low resistance metal to metal contact.

**Fabrication:**
The device is fabricated with a single step patterning that precisely places source, drain and gate perfectly aligned with the nanopillar. Devices employ a variety of tricks to decrease the critical dimensions (Figure 2). Stiction-free processing can be achieved using an isotropic SF6/O2 etch. A key feature of the fabrication is the thin Si3N4 insulating spacer. The Si3N4 enables low voltage operation by making possible independent optimization of gap and pillar sizes. Therefore, pillars can be reduced while maintaining small gap sizes.

Gaps were a conservative 200-350 nm for our devices. Starting with larger gaps enables deeper etching for taller pillars and reduces the likelihood of stiction during wet processing. Gap reduction is easily achievable by longer blanket evaporation of metal in the final process step. Electrical isolation is maintained between the body and the other electrodes by virtue of the silicon undercut beneath the Si3N4.

**Results:**
Operation of a typical device at 10V in air is shown in Figure 3. It has a gap of ~ 230 nm measured from the S/D, and non-uniform pillar thickness ~ 130 nm at the bottom and ~ 180 nm at the top. Figure 4 shows the measured device after pull-in is achieved.

**References:**