A Study on Ferroelectric Properties of Vanadium Dioxide Film

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Abstract:

We report that vanadium dioxide (VO$_2$) acts similar to a ferroelectric material when sandwiched between two silicon dioxides. VO$_2$ memory devices had hysteresis properties in response to gate voltage, and the direction of threshold voltage shift was opposite to that of charge trapping. The memory window was about 1V when a gate voltage was cycled between -4 and 4 V. Remnant polarization and coercive field were about 0.53 µC/cm$^2$ and 450 kV/cm, respectively, which were extracted using the saturation phenomena of threshold voltage shift. The state decayed gradually due to depolarization field and retention time was around 15 minutes at room temperature.

Summary of Research:

VO$_2$ is a representative correlated oxide material with phase transition close to room temperature [1]. It has also very fast transition time, about order of pico-second [2]. As is well known, vanadium has various oxidation states of +2, +3, +4, and +5. Among them, V$_2$O$_5$ is the most stable and common oxide compound, which is a ferroelectric material with the Curie temperature $T_c = 230^\circ$C [3]. VO$_2$ has a distorted rutile structure in which the vanadium ion has moved away from the center of the oxide octahedron. The lengths of the long and short bonds in VO$_2$ are 2.03, 2.01, 2.05Å, and 1.86, 1.87, 1.76Å, respectively [4]. However, the ferroelectric-like property of VO$_2$ has not been studied so far, because its metal-insulator phase transition property has received more attention.

In our experiment, ferroelectric memory devices with VO$_2$ floating gates were implemented using conventional CMOS processing technology. The device structure is composed of a transistor with a gate structure of metal-insulator-ferroelectric-insulator-semiconductor (MIFIS), where the VO$_2$ film is employed as an intermediate layer. VO$_2$ is sandwiched between thermal SiO$_2$ and ALD SiO$_2$ on a p-type silicon wafer. An active area is defined by i-line lithography, and arsenic implantation to define source and drain regions was employed at a dose of $3 \times 10^{15}$ cm$^{-2}$. After annealing the wafer, thermal silicon dioxide (30 nm) was grown, followed by the deposition of sputtered VO$_2$ film (200 nm) and 110$^\circ$C plasma ALD process for SiO$_2$ dielectric layer (60 nm). A Ti/Al metal gate was evaporated for the lift-off process.

Figure 1 shows the hysteresis behavior of gate capacitance in response to gate voltage. As the gate voltage was cycled between ±4, ±6, ±8, and ±10 V, the capacitance cycled counterclockwise and the memory window increased linearly according to the cycling range of the gate bias. This hysteresis behavior is consistent with ferroelectric polarization switching and contrary to the hysteresis resulted from charge injection. As shown in Figure 2, the
threshold voltage shift was saturated as the sweeping range of the gate bias was 20 V, which means that the polarization of VO$_2$ reached at its maximum value. That is, at that point, the saturation field was given to the VO$_2$ layer and so we can extract the remnant polarization of VO$_2$ from the threshold voltage shift at the sweeping gate voltage of 20 V, which is around 0.53 µC/cm$^2$. This value is more than one order of magnitude higher than the minimum polarization for a FeDRAM [5].

After application of the saturation field to VO$_2$, we measured the hysteresis in response to gate voltage to extract the coercive field of VO$_2$. As shown in Figure 3, the average gate voltage of forward and backward sweep when $C_g = 2$ pF was saturated as the cycling range of gate bias reached at 5 V. This means that when the field input to VO$_2$ is below the coercive field, the threshold voltage is still higher due to the remnant polarization, and when the field is over the coercive field, the average threshold voltage should be stabilized because the remnant polarization was removed whenever the gate voltage was cycled. Therefore, the coercive field of VO$_2$ is around 450 kV/cm$^2$.

Figure 4 shows the data retention characteristics. After applying the gate pulse, we subsequently measured the gate capacitance at zero gate bias to get rid of the measurement effect. The retention time after giving 10 V gate pulse was worse than after giving 20 V gate pulse, which may be caused by the polarization instability of unsaturated ferroelectric film. In case of 20 V gate pulse, the retention time is around 15 minutes, which is three orders of magnitude longer than the current generation of conventional DRAMs.

References: