A Ferroelectric and Charge-Based Hybrid Nonvolatile Memory

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Abstract:
We introduce a new nonvolatile memory that incorporates ferroelectric (FE) switching layer and charge-storage floating node in a single gate stack. This hybrid FE-charge design reduces the depolarization field [1] in the FE layer as well as increases the memory window over conventional FE-FET. The magnitude of the electric field in the tunnel dielectric is reduced at retention and enhanced at program/erase from the FE polarization. This work discusses the working principle, gate stack design, fabrication and experimental results of this hybrid design compared to FE-FET and charge-trap Flash.

Device Concept and Working Principle:
Figure 1 shows an example of experimental design for the gate stack and program/erase (P/E) operation of the hybrid cell. A floating gate (FG) (discrete/continuous) is included above the FE layer. A thin top oxide serves as a tunnel barrier for gate injection and removal of electrons [2]. Program condition ($V_{\text{PROG}} < 0$) orients FE polarization with positive surface charge facing the gate and hence increases the $V_{\text{TH}}$ of the cell. The injected electrons into the FG add to the $V_{\text{TH}}$ shift. These electrons also stabilize the positive dipole charge on FE during retention and thus decrease the depolarization field. Erase operation ($V_{\text{ERASE}} > 0$) removes the electrons from FG and reverses the polarization of FE layer.

Fabrication and Experimental Results:
0.5% solution of 70:30 P(VDF-TrFE) in MEK was spun-coated and annealed at 140°C for 10 minutes [3] to obtain a film thickness of 35 nm above the bottom oxide. Subsequent processing of the hybrid device was limited below 110°C.
Control FE-FET and gate inject (GI) Flash devices with the same corresponding FE layer and tunnel oxide thicknesses and identical EOTs were also fabricated for comparison.

Hybrid devices showed larger $\Delta V_{FB}$ against FE-FET for $V_{PROG} > 10$ V due to injected-electron contribution as seen in Figure 2. Figure 3 estimates the injected electron density and contribution of FE switching to $\Delta V_{FB}$ in hybrid devices.

GI Flash showed poor $\Delta V_{FB}$ due to lesser tunnel oxide fields compared to hybrid devices. Reduced depolarization field improves retention in hybrid devices over FE-FET as seen in Figure 4. GI Flash also demonstrated limited retention due to inferior quality of top oxide constrained by present process integration. Hybrid device showed $> 10^4$ s retention and can present significantly better results with improved quality tunnel barrier. During program, large amount of charge is trapped in the polycrystalline PVDF film. This charge gradually leaks out to the gate with minimal positive bias in FE-FET thereby limiting effective retention time of the device. The existence of the trapping layer in hybrid design provides an ideal sink to this leak path. Trapped charge in the FE layer is emitted to the trap layer assisted by the depolarization field.

**Summary of Research:**

We propose a new highly scalable hybrid nonvolatile memory designed with ferroelectric PVDF film and HfO$_2$ charge-trap layer that takes advantage of low-voltage operation from FE-FET as well as reduces depolarization field by gate-injection of charge.

**References:**