Microring-Based Optical Pulse Train Generator

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Abstract:

Recently, we developed the concept of a new optical pulse train generator, based on microring resonators and the circuit technique of time interleaving. Here we report the experimental demonstration of a four-tap prototype fabricated on silicon-on-insulator (SOI) substrate.

Summary of Research:

Microrings have become one of the critical building blocks in silicon photonics due to their ultracompact size, which enables large-scale electronic photonic integrated circuits (EPICs) to be foreseen in the near future. To overcome the fundamental challenge of the large potential bandwidth of photonics but the significantly lower speed of electronics in EPICs, we would like to explore microring-based EPICs more in their time domain properties and applications instead of many other wavelength-division multiplexing (WDM) approaches.

Recently, we proposed a new microring-based optical pulse-train generator (M-OPTG) [1], as shown in Figure 1. Multiple microrings are coupled to the input trigger waveguide in series, and are used as compact couplers to divide the input pulse into multiple pulses. Meandering waveguides are inserted between stages as optical delay lines to introduce large stage delays, which determines the timing of the output pulses. The amplitude of the output pulses is controlled by the coupling coefficient of the microrings in each stage. Finally, the stage outputs are symmetrically combined to form a pulse train in the output waveguide. A four-tap, first order prototype is designed and fabricated on SOI substrate. We use rectangular ring resonators to control the stage coupling by changing the coupling lengths $l_1$ as shown in the inset of Figure 1. A test circuit without output combiner is also fabricated to measure each stage output separately.

To fabricate the device, we start with the SOI wafer, which has 250 nm thick top silicon and 3 mm thick buried oxide. Electron beam lithography is used to pattern all the structures due to the submicron waveguide cross section. The circuit patterns are then transferred to the top silicon layer by chlorine reactive ion etching (RIE). Thermal oxidation is then applied to further smooth the sidewalls. Finally, oxide cladding is deposited using plasma enhanced chemical vapor deposition (PECVD). The circuit is checked under scanning electron microscopy (SEM) after Si etching. As we can see from Figure 2, ring resonators with larger coupling length $l_1$ are used in the latter stages for a larger stage coupling. A close-up SEM image of the ring resonator in the first stage is also shown in the inset.
Figure 3 shows the results of initial time-domain measurement of the test circuit with separate stage outputs. Due to the limited 20 GHz optical bandwidth of our oscilloscope, the measured pulse width is broadened from about 20 ps to about 40 ps. However, the stage delay, which is measured as the timing between the output pulse peaks, is quite uniform for all the stages as shown in the inset of Figure 3. The stage delay is designed to be 25 ps and measured as 30 ps. The output pulses from the latter stage are smaller than the former ones, especially for the fourth stage. This is caused by the waveguide propagation loss as well as the shift of the resonant frequency of the microrings. Therefore, post-fabrication thermo-optic (TO) or electro-optic (EO) tuning capabilities are needed to improve the circuit performance.

To conclude, we demonstrate the prototype implementation of a four-tap, first order M-OPTG. Test circuit with uncombined outputs shows correct timings of the four output pulses with stage delay of 30 ps.

References: