Abstract:

Integration of photonics with electronics, although common in academic research, still fails to be commercialized due to the incompatibility of materials and processes of simple photonics. Utilizing CMOS-compatible materials and processes, we develop a multi-layered backend process to integrate silicon photonics using low temperatures on a pre-existing electronics stack. We achieve losses of ~1 dB/cm in the L-band, -0.04 dB waveguide crossings and 24 dB extinction frequency filters.

Summary of Research:

Advances in silicon and silicon-compatible photonics have spurred intense research in the area of optical interconnects, where it could potentially be used to increase the bandwidth and lower the power of computing systems such as multi- and many-core processors [1,2]. Unfortunately, densely integrated silicon photonics with microelectronics has yet to emerge commercially. While there may be clear advantages over electronic communication, the integration of photonic interconnects with on-chip electronics requires a costly change to well-established complimentary metal-oxide-semiconductor (CMOS) processes.

Multilayer photonics can go beyond simple integration, providing interesting advantages to the system as a whole. Single layer interconnect photonics is typically criticized as not providing enough performance gain in terms of bandwidth and power, to justify the integration challenges. Losses from waveguide crossings for example, a necessary limitation of single layer optical networks, are often cited as one of the biggest obstacles in these systems [3]. A multilayered system could reduce or eliminate these restrictions altogether by avoiding physical crossings. We would also give architects a new dimension to explore, perhaps leading to denser as well as more complex networks with radically higher cross-sectional bandwidth and reduced communication power consumption.

Along with using group IV compatible materials, the most important detail in backend photonics is using processes around or below 400°C to avoid distressing the metallization and changing the dopant diffusion. Our fabrication uses plasma enhanced chemical vapor deposition (PECVD) of all layers, planarization to allow for vertical stacking, and proper patterning and spacing of structures to allow for coupling and insulation. We work with Si₃N₄ as a guiding medium for its good optical characteristics. Si₃N₄ is readily found in CMOS for passivation, masking and dielectric layers and provides lower optical losses than c-Si in the NIR [4] when using SiO₂ cladding, also a CMOS dielectric.

We demonstrated the waveguide loss to be just over 1 dB/cm for most of the L-band in our 400 nm × 1 µm geometry Si₃N₄. The loss increases steadily into the C-band due to Si-H and N-H bonds in the film [5]. These losses are comparable to those shown in the literature for silicon nitride and are still better than most comparable silicon single-mode waveguides [4]. We measure losses for the waveguide crossings to be -0.04 ± 0.002 dB/cross for waveguides separated vertically by 800 nm. Lastly we test the optical path through the vertically-coupled filter and measure a channel bandwidth of 25 GHz and an extinction ratio of -24 dB. Figure 2 shows both the drop port and through port normalized by the input power to the device. We also measure an insertion loss of -0.6 dB from the drop port response, and we calculate the loaded quality factor of the resonator from the linewidth to be $Q_L = 7.5 \times 10^3$ and estimate an ideal intrinsic value of $Q_i = 1.7 \times 10^5$. 
References:


Figure 1: Fabricated device; (a) microscope image of bus waveguides and microring resonator, (b) vertically coupled structure with TE mode and geometry parameters, (c) false color SEM image of ring cross section, and (d) close-up SEM of silicon nitride waveguide cross section.

Figure 2: Results of fabrication; (a) propagation losses of PECVD Si$_3$N$_4$ waveguides (400 nm x 1000 nm) over wavelength of interest, (b) averaged loss per vertical crossing (800 nm separation), and (c) microring resonator (30 µm radius) through and drop port responses from both layers.