The performance of $\text{Al}_x\text{In}_{1-x}\text{N}/\text{GaN}$ high-electron-mobility transistors (HEMTs) fabricated on silicon carbide (SiC) substrates is reportedly demonstrated. Transconductance of 530 mS/mm with peak current density 1.4 A/mm is achieved. When driven at 10 GHz CW, output power of 4 W/mm with 43% PAE is observed.

Summary of Research:
$\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high-electron-mobility transistors (HEMTs) are well-suited to high-frequency and high-power applications [1,2]. HEMT frequency scaling, by reducing the gate footprint, is not in itself sufficient to achieve high power performance at increasing frequency. The unity-current gain frequency is inversely proportional to the effective gate length,

$$f_T = \frac{v_{\text{eff}}}{2\pi L_{G,\text{eff}}} \approx \frac{v_{\text{eff}}}{2\pi (L_{G0} + 2d)},$$

where $v_{\text{eff}}$ is the effective electron velocity in the gallium nitride (GaN) channel, $L_G$ is the gate length, and $d$ is the barrier thickness between the gate footprint and the two-dimensional electron gas (2DEG).

In order to maintain effective gate modulation and mitigate short channel effects, when reducing gate length, it is necessary to simultaneously reduce the barrier thickness [3]. To maintain a desirable current density, on the order of 1 A/mm, a thinned barrier dictates an increase in aluminum (Al) composition. Engineered high-Al composition $\text{Al}_x\text{In}_{1-x}\text{N}$ barriers provide higher polarization induced sheet charge with lower strain than achievable using traditional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layers. In this work, the performance of $\text{Al}_x\text{In}_{1-x}\text{N}/\text{AlN}/\text{GaN}$ epitaxial layers was grown by metalorganic chemical vapor deposition (MOCVD) on 3″ SiC substrates. The 1.85 µm GaN buffer was compensation doped with iron to increase its resistivity and mitigate subthreshold leakage current. The buffer was topped by a 15 Å AlN interbarrier and an 80 Å $\text{Al}_{0.8}\text{In}_{0.2}\text{N}$ barrier.

The barrier composition was chosen to be Al-rich compared to lattice-matched $\text{Al}_{0.18}\text{In}_{0.82}\text{N}/\text{GaN}$ case, thus leveraging piezoelectric polarization to further enhance the sheet charge density, $n_s$, of the 2DEG.

The surface morphology was characterized by atomic force microscopy (AFM). The 2DEG properties were examined by wetted Hg probe C-V, Lehighton, and transfer length method (TLM) measurements.

The devices were fabricated at the Cornell NanoScale Science and Technology Facility. A standard Ta/Ti/Al/Mo/Au ohmic contact recipe was used. Mesa isolation was achieved via a Cl$_2$/BCl$_3$/Ar ICP etch following the 800°C ohmic contact anneal. The wafer was passivated with 45 nm plasma enhanced chemical vapor deposition (PECVD) SiN$_x$ at 375°C, which was etched by CF$_4$ and field-plated, Γ-shaped Ni/Au gates were deposited.
TLM measurements were performed using the four-point probe technique. Direct current (DC) characterization and small-signal measurements were completed using on-wafer GSG probes. Power-matched large-signal measurements were made using a Maury load-pull system at 10 GHz CW.

AFM measurement of the Al$_x$In$_{1-x}$N surface indicates an RMS roughness of 0.6 nm for a 10 µm scan. The 2DEG density is measured by C-V at multiple sites on the wafer as $n_s = 2.2 \times 10^{13}$ cm$^{-2}$. Excellent agreement is observed with a Schrödinger-Poisson model of the epitaxial layers.

Leighton measurements mapped across the 3″ wafer prior to processing indicate $R_{sh} = 252.6 \pm 16.2 \, \Omega/\square$. This is in good agreement with TLM results for the SiN$_x$-passivated Al$_x$In$_{1-x}$N material, presented in Table 1 alongside data from a 20 nm-Al$_{0.26}$Ga$_{0.74}$N/GaN-on-SiC wafer, which was processed in parallel.

A study of anneal temperatures 740°C-820°C in 20°C increments confirms optimal contact formation at 800°C, which is used for the devices in this work.

Considering a representative 2 × 50 µm HEMT with $L_{GD} = 1.5$ µm, peak DC metrics include $I_{D0} = 1.03$ A/mm, $I_{D|+1Vgs} = 1.37$ A/mm, and $g_m = 530$ mS/mm (Figure 1).

For this device with a 0.15 µm field-plated gate footprint, the unit-current-gain frequency $f_t = 37$ GHz, and breakdown onsets at 37 $V_{DS}$ and is preceded by an increase in gate current.

The SiN$_x$ passivated devices exhibit ~ 20% drain lag in the knee region when driven with 500 ns pulses at a low duty cycle from $V_{DSq} = 20$ V and $V_{G Sq} = -5$ V. Inhibited by DC-RF dispersion and restricted by breakdown to 20 $V_{DS}$ bias, output power in deep class AB operation driven at 10 GHz CW is 4.0 W/mm with 43% PAE.

Al$_x$In$_{1-x}$N/GaN epitaxial layers on a high-thermal conductivity substrate such as SiC are a promising platform for achieving efficient, high power, high frequency operation. The thinner barrier facilitates scaling device geometries well into the mm-wave regime.

Compared to typical Al$_x$Ga$_{1-x}$N/GaN device values, the relatively poor ohmic contact even at an optimized anneal temperature prompts a contact metallization study for high-Al composition, wider bandgap Al$_x$In$_{1-x}$N barriers. It is observed that channel breakdown is seeded by an increase in hot electrons tunneling through the sharp Al$_x$In$_{1-x}$N barrier; this motivates the in situ growth of a GaN cap layer [4] or the deposition of a thin gate dielectric [5] to reduce the tunneling probability.

References:


Abstract:

Trap-based floating gate flash memory is a viable alternative to conventional poly-Si floating gate memory primarily due to its immunity towards stress induced leakage current in the tunnel oxide. This work provides a systematic study of the effect of ordered porosity in charge trapping layer. Memory gate stacks with nanopores (NPs) in aluminosilicate trapping layer were fabricated by block copolymer self-assembly process. NP device characteristics benchmarked by C-V measurements against those without NPs, exhibit enhanced tunneling efficiencies and longer retention of the stored charge.

Device Concept:

Consider a memory gate stack with ordered NPs above the tunnel dielectric [1]. The NPs perturb the electric field in the surrounding medium, diminishing the intensity in the regions facing the electrodes (gate/substrate) and enhancing it in regions between the pores. Figure 1 depicts the vertical electric field on various cut lines through such gate stack for the program condition. The enhancement of electric field in SiO₂ can be about 25% and is expected to be larger for high-κ dielectrics. This inhomogeneity therefore favors electron capture preferentially between the pores, possibly pinning their capture location. Although the EOT reduces, carrier injection efficiency can improve in regions between the NPs. A shorter tunneling distance enables faster capture of injected charge.

Fabrication and Experimental Results:

Devices were fabricated on a spin coated porous aluminosilicate (80% SiO₂, 20% Al₂O₃) thin film (thickness ~ 10-12 nm) generated through block copolymer self-assembly [2]. A capping layer of 5 nm Al₂O₃ was deposited before calcining (organic removal by thermal treatment) the film to preserve the porosity. Figure 2 is the SEM image
of the calcined film (without the capping layer) revealing ~ 8-10 nm diameter NPs in aluminosilicate matrix. Memory structures with thermal SiO$_2$ and ALD Al$_2$O$_3$ as tunnel dielectric were fabricated along with the corresponding control samples (without NPs). The spin-on aluminosilicate film also acts as a trapping layer and is seen to favor electron capture. Control samples were seen to have a larger $\Delta V_{th}$ than samples with NPs possibly on account of their larger trapping volumes. Varying pulse time measurements were performed on devices to estimate efficiency of electron injection.

Figure 3 illustrates $\Delta V_{th}$ against program pulse time ($t_{prog}$) for NP and control samples with SiO$_2$ tunnel dielectric. Both samples were seen to have the same initial flat band voltage ($V_{FB}$). Further, as expected, NP samples were seen to have a higher EOT (inset) due to the low-k NPs in the trapping layer. Electron injection in NP samples was seen to be more efficient than the control samples for smaller $\Delta V_{th}$. This validates improved injection in inhomogeneous NP trapping medium. At longer $t_{prog}$, the control samples were seen to catch up in $\Delta V_{th}$ due to their significantly higher trapping volume. Figure 4 shows retention measurements on the same structures. Electrons trapped in NP samples observe a higher effective barrier to escape therefore prolonging their retention in the captured location.

Summary of Research:

We present a systematic study of porosity in the memory gate stack and its influence on performance characteristics. Porosity alters the electrostatics crucial to program efficiency and retention behavior and is seen to offer certain advantages. Engineered nanopores may help improve our understanding of carrier capture in amorphous dielectrics.

References:

Abstract:
The self-assembled monolayer (SAM) of ferrocenecarboxylic acid (FcCOOH) and 5-(4-carboxyphenyl)-10,15,20-triphenyl-porphyrin-Co(II) (CoP) with high-$k$ dielectric were integrated into the Flash memory gate stack. Asymmetric charge injection behavior was observed, which can be explained by Fermi-level pinning between the molecules and the high-$k$ dielectric. Engineering the HOMO-LUMO levels with different redox molecules may help realize a multi-bit memory cell with less variation.

Device Concept:
The molecular redox state is used as charge storage to reduce variations observed in memory with discrete storage nodes [1,2]. Through the program/erase (P/E) operations over tunneling barriers, the device structure also provides a unique capability to measure the redox energy without the orbital hybridization of electrodes in direct contact.

Fabrication and Experimental Results:
The schematics of the devices with FcCOOH (S1) and CoP (S2) are illustrated in Figure 1. After 2.2 nm or 3.0 nm dry thermal oxide was grown on a p-type (100) silicon substrate, the wafer was immersed in a solution of dimethyl formamide (DMF) mixed with FcCOOH to form a 1 mM solution. The solution was kept at 80°C for 120 minutes under argon environment during the self-assembly process. As illustrated in Figure 2, hole injection is preferred when FcCOOH is embedded in Al$_2$O$_3$, which can be explained by the Fermi-level pinning theory [2]. The charge neutrality level (CNL) can be regarded as the local Fermi-level of Al$_2$O$_3$. The band diagrams with FcCOOH embedded in Al$_2$O$_3$ is illustrated in Figure 3. Upon injection, electrons would preferentially relax to the interface traps near the CNL with lower energy for FcCOOH. On the contrary, electron injection shows two distinct levels of Coulomb staircase for CoP as illustrated in Figure 4. The amount of flatband voltage shift ($\Delta V_{FB}$) is 1.32 V for a CoP number density of $2.2 \times 10^{12}$ cm$^{-2}$ assuming single electron injection, which corresponds well with the $\Delta V_{FB}$ of 1.4 V measured at room temperature. Although the CNL and HOMO-LUMO energy levels of CoP$^{1+}$...
is unknown after interface formation, we expect the CNL to be in close proximity with LUMO so that the injected carriers will not have the tendency to relax to interfacial trap states.

**Summary of Research:**

We have successfully integrated a monolayer of redox molecules in a Flash memory device structure using solution based self-assembly technique and demonstrated three programmable molecular orbital states of CoP, including CoP\(^0\), CoP\(^1\), and CoP\(^2\) at room temperature, which may help realize step charging into a multi-bit memory cell. With the abundant choices of redox molecules and their inherent mono-dispersion in size and energy levels, our proposed approach can be readily integrated into a MOS-based nonvolatile memory cell and pave the wave for realizing multilevel molecular memories.

**References:**


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Figure 3: Energy band diagram representation of FcCOOH capacitor structure. The charge neutrality level (CNL) of Al\(_2\)O\(_3\) is shown, and FcCOOH is assumed to be at its neutral state.

Figure 4: (a) HFCV and (b) $\Delta V_{FB}$ as a function of the programming voltage at 10 Kelvin and room temperature for CoP. The programming voltage ($V_p$) for electron and hole charging is applied from 0 V to +42 V and 0 V to -18 V, respectively.
Abstract:
This project is focused on the fabrication of an electronic Y-Branch Switch (YBS), which utilizes the wave nature of electrons to allow for fast switching and low power operation. Electron waveguide devices are required to be smaller than the electron mean free path to allow for ballistic carrier transport. We have developed a fabrication process that uses electron beam lithography to achieve small device sizes that are transferred into III-V quantum well based heterostructures. Quantum wire waveguides were fabricated using a SiN hard mask and anisotropic etching techniques to create trenches that isolate the device structure from the surrounding 2D electron gas.

Summary of Research:
An analysis of the Y-Branch Switch was first proposed by Palm and Thylén in 1992 [1]. It was shown that when operating such a device under single mode coherent transport, there is no theoretical thermal limit for switching energy. The switching voltage is related to the transient time of the electron through the branching region and does not depend on drift and diffusion. In this switching mode, the voltage required to turn the device ON and OFF is in the millivolt (mV) range. Other types of YBS operation also exist that have been realized at room temperature, including self gating at low currents and nonlinear ballistic multimode transport [2]. These devices show promising characteristics that may be capable of a variety of low-power logic applications.

The device layout of the YBS (Figure 1) has a one dimensional channel that branches off into two drain output channels. By applying a transverse external gate voltage across the central branching region, electrons can be guided into either of the two drain outputs depending on the direction of the field. The gate potential modifies the wavefunction of the electron and shifts the probability distribution towards one of the two possible outputs.

Our devices consisted of a GaAs/AlGaAs quantum well heterostructure grown on a GaAs substrate using molecular beam epitaxy. The two dimensional gas formed at the GaAs/AlGaAs interface is located approximately 50 nm below the top surface of the wafer. Delta doping was used in the top AlGaAs barrier to limit any cumbolic scattering from ionized impurities that may degrade carrier mobility. A 50 nm thick SiN hard mask was deposited using plasma enhanced chemical vapor deposition (PECVD). PMMA resist was then patterned with the JEOL 9300 electron beam lithography tool. A CHF₃ anisotropic plasma etch was used to transfer the YBS pattern from the resist to the silicon nitride hard mask. The sample was then etched in chlorine-based plasma to a depth of ~ 1 µm (Figure 2) to form the electron waveguide mesa with vertical sidewalls.
Device sizes ranged from 40 nm to 200 nm with a constant branching angle of 60 degrees. The remaining SiN was then removed and optical lithography of the III-V n-type Ohmic contact regions was carried out. Electron beam evaporation was used for palladium germanium deposition. A final large trench isolation step was carried out using photolithography and chlorine based plasma. This region overlapped the electron beam patterned trenches and assured that was no leakage current flowing between the gate (the surrounding two dimensional gas) and either of the two branches and also between the branches themselves.

We are currently in the early stages of electrical testing and characterization of the YBS and expect to see switching at frequencies in the 40 GHz range and a low switching voltage of ~ 1 mV. Operation at liquid helium temperatures will allow us to probe the lowest energy modes available for phase coherent electron transport. Room temperature electrical testing of the YBS as a transistor will be carried out, as well as investigating the self gating effect. Other quantum well heterostructures are being considered for fabrication, including a higher mobility InGaAs quantum well device and a YBS using antimonide based III-V structures for hole transport. Optimization of growth parameters such as sheet carrier concentration and quantum well placement from the surface will also be needed.

References:
Single Element Phase Transition Memory

CNF Project # 804-99
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Abstract:

We propose a fast single element non-volatile memory made by coupling phase transition property changes to a transistor channel. Our device has the same structure as a cell transistor of Flash memory. In the place of floating gate, we put a phase transition material, which can change its phase in response to current flow in the channel inducing gate stack temperature changes. So, we can store information by coupling phase transition, not by direct charge transport. Then, we expect that we will reduce power consumption and overcome a variety of retention and reliability issues of the conventional memories.

Summary of Research:

As is known to all, DRAM and Flash are the most popular memory devices. However, they have some shortcomings. For example, DRAM is a volatile memory, so it needs to refresh its data periodically and then it has more power consumption. Meanwhile, Flash has slow write and erase time and limited write endurance. Therefore, a lot of research has been done to make a universal memory, which can have DRAM and Flash’s merits together. Our research started from that point.

In addition, power dissipation is one of the most critical issues in making devices [1,2]. As the device size shrinks to nanoscale, that issue comes to be more crucial and intrinsic. Then, what if we make a device that can store information without charge transport to its memory node?

So, we propose a novel single element memory device using a phase transition material, of which the phase change is coupled with its transistor channel and then we can use dissipated thermal energy in writing data and information can be stored without any charge transport to a memory node.

Our device has the same structure as the cell transistor of Flash, so its cell consists of one transistor only. In the place of floating gate, we put a phase transition material, which can change its phase in response to current flow in the channel inducing gate stack temperature change. While flowing the channel current, the joule heat occurs and can be transferred to the phase transition material via the bottom oxide. If this transferred thermal energy is enough to switch the phase, the transistor can have a different property from the initial one due to the variation of equivalent oxide thickness. This variation results from the change of the dielectric constant induced by the phase transition.

In our experiments, we used Ge$_2$Sb$_2$Te$_5$ (GST) as a phase transition material and made a transistor with a bulk silicon substrate. Figure 1 shows the resistance change of GST after external heating and cooling. According to adapting process steps, the initial resistances of GST are different.

Figure 1: GST resistance change after heating and cooling.
GST in the metastable fcc crystalline phase. It tells us that the fabrication processes can make an effect on the initial phase of GST. Considering that the critical temperature of amorphous to fcc crystalline transition is around 150°C, we should control all the processes under 150°C.

After H₂ anneal at 300°C in flowing 5% H₂ for 1 hr, the resistance decreased to about 300 Ω, which is close to the value of GST in the hcp crystalline phase. Once the phase of GST became hcp crystalline, thermal hysteresis behavior disappeared and GST acted like a metal. That is, when the temperature increased, the resistance also increased due to the increase of phonon scattering.

Before measuring the effect of joule heating, we investigated the threshold shift and capacitance change according to the external heating. As shown in Figure 2, after H₂ anneal, the threshold voltage decreased and gate capacitance increased. It shows that the dielectric constant of GST changed due to its phase transition. Unlike the results of external heating, the effect of joule heating was a little bit small and relatively not reproducible as shown in Figure 3.

As mentioned before, we made a transistor with a bulk device structure. In that case, heat generated in the channel can dissipate through the substrate more easily than be delivered to a PT material through the gate oxide, because the thermal conductivity of silicon is about 150 times higher than that of silicon dioxide. Therefore, the temperature of the channel and the heat delivery efficiency must be lower than expected.

To overcome these issues, we are going to make a new transistor with a wire-based device structure as shown in Figure 4. This transistor has a suspended channel with an air-gap, of which the thermal conductivity is around 0.025 W/mK, 1/40 of that of silicon dioxide. We expect that this new transistor with high thermal impedance due to the air-gap should have more efficient heat delivery to the PT material. The new high thermal impedance structures should overcome these shortcomings, and if successful, and if reliability is still achievable, this embodiment may be an appealing medium power and medium speed non-volatile memory alternative suitable for embedded and stand-alone applications.

References:
Graphene / Carbon Nanotube Cross-Junction Devices

CNF Project # 900-00
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Abstract:

We engineer an electrically contacted graphene/carbon nanotube junction using graphene grown by chemical vapor deposition (CVD) and aligned arrays of CVD-grown carbon nanotubes. We employ electrical transport measurements to show that the two materials make good contact over a length scale of 1 µm, with a total junction resistance on the order of the carbon nanotubes’ resistance over 1 µm. Our results suggest that it should be possible to use graphene as the contacts and carbon nanotubes as the active element in a transparent, flexible, carbon-only transistor.

Summary of Research:

Despite extensive research into the properties and applications of both graphene and carbon nanotubes (CNTs) over the last decade, fabrication challenges have prevented the scientific community from studying electronic interactions between the two materials. Here we draw on recent advances in the creation of both large-area, single-layer CVD-grown graphene [1] and aligned arrays of parallel CNTs [2] to explore the junction between the two materials.

Fabrication of our devices is demonstrated in Figure 1. We begin by growing single-layer graphene by chemical vapor deposition on a copper film [1], and transfer the film onto an Si/SiO2 chip as in Ref. [1]. The graphene is then patterned with optical lithography into strips of varying width (here, 2-9 µm), and metal electrodes (2 nm Ti, 50 nm Pt) are formed by photolithography and electron-beam evaporation (Figure 1(a)). In parallel, we grow aligned arrays of carbon nanotubes on y-cut, single-crystalline quartz wafers by CVD [2], resulting in arrays with an average density of 1-2 CNTs/µm, in a mixture of metallic and semiconducting nanotubes with an average diameter between 1-3 nm. We cover the nanotubes with 100 nm of evaporated gold and two layers of a commercially available water-soluble poly-vinyl alcohol (PVA) tape as a transfer medium (Figure 1(b)). The CNT/Au/PVA film is peeled up by hand, and can be placed in the desired orientation and location on the graphene device (Figure 1(c)). The transfer materials are removed, and as a final step, the graphene and nanotubes are lithographically patterned into a cross shape to prevent unwanted electrical contacts (Figure 1(d) and Figure 2).

To eliminate contact resistance and other series resistances from our electrical readings, we make use of four-point-probe measurements, which allows us to measure a graphene intrinsic resistance of 1-1.2 kΩ/square. We can similarly measure the intrinsic resistance of each segment of the CNTs, rNT, which range from 5-100 kΩ/µm. Finally, we arrange the electrodes as in Figure 2 to measure the four-point resistance of the graphene/CNT junction, and observe junction resistances in the range of 200Ω-5kΩ, suggesting an exceptionally good contact.

However, in analyzing these results, we must carefully consider the fact that the contact extends over some finite length. The system is modeled in the transmission line circuit of Figure 3 [3]. In such a geometry, voltage measurements at the end of

Figure 1: Fabrication. (a) Grow single-layer graphene by CVD; transfer to Si/SiO2 wafer. Pattern graphene and electrodes. (b) Grow aligned arrays of CNTs on y-cut quartz. Cover with 100 nm Au and two layers of PVA tape, and peel up PVA/Au/CNT film. (c) Place film in preferred orientation on graphene device. (d) Remove PVA and Au. Etch away excess CNTs to prevent unwanted contacts.
a transmission line must be analyzed in the context of the complete circuit. The correct analysis [3] in the series limit gives the expression shown in Figure 3, for the measured resistance as a function of the contact conductance $g_c$.

A plot of $r_{NT}$ versus $1/g_c$ for all working devices is shown in Figure 4, plotted along with a line of slope 1. The apparent one-to-one correspondence of the two values, which differ in their units, implies that the characteristic length of the contact is on the order of a micron.

We can define this value as $l_c = \sqrt{1 / r_{NT} g_c} = 1 \mu m$. This result is strikingly similar to that of the resistance between the consecutive layers of a multi-walled carbon nanotube, where the exponential decay length is on the order of 1 $\mu m$ [4]. The feasibility of device applications of a new material will of course also be determined by the two-point resistance of a sufficiently large contact, $R_c$, and here we see that for a contact of $L > l_c$, the resistance should be given by $R = r_{NT} l_c$. For all devices, this is on the order of the CNT intrinsic resistance over a length of 1 $\mu m$.

In conclusion, we have succeeded in fabricating graphene/carbon nanotube cross junction devices which demonstrate that graphene and CNTs make good contact over a length scale of about 1 $\mu m$, and that the total contact resistance of a micron-long contact is on the order of the nanotube intrinsic resistance over 1 $\mu m$. These measurements and fabrication advances demonstrate the feasibility of a flexible, transparent, all-carbon transistor in the immediate future.

References:
Al$_x$Si$_y$N$_z$ Passivated AlGaN/GaN High Electron Mobility Transistors

CNF Project # 1230-04
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Abstract:

AlGaN/GaN high electron mobility transistors (HEMTs) passivated with LPCVD Si$_y$N$_z$ and Al$_x$Si$_y$N$_z$ were fabricated side-by-side, and their performance compared in DC, small-signal, and large-signal test environments. Al$_x$Si$_y$N$_z$ passivated devices measured a reduced dependence of source resistance with drain current density, 1.5 x the breakdown voltage, and an increased microwave output power and power added efficiency when compared to similarly sized Si$_y$N$_z$ passivated devices.

Summary of Research:

AlSiN was explored as a passivation for AlGaN HEMTs due to its greater bandgap and its expected lower permittivity at microwave frequencies. The increase in bandgap is evidenced by its lower infrared (IR) index of refraction when compared to Si$_y$N$_z$ as measured by ellipsometry (Figure 1). Al$_x$Si$_y$N$_z$ and Si$_y$N$_z$ films were deposited in a modified low-pressure chemical vapor deposition (LPCVD) system onto mesa-isolated AlGaN/GaN HEMT structures with 250 Å Al$_{0.30}$Ga$_{0.70}$N barriers grown on S.I. SiC. Dielectric deposition was performed at 750°C at a pressure of 2 Torr with trimethyaluminum, dichlorosilane, and ammonia as precursors [2]. The aluminum fraction of the deposited dielectric was measured to be ~ 12 at.% by x-ray photoelectron spectroscopy. Si$_y$N$_z$ passivated structures had a full channel charge of ~ 1.6 x 10$^{13}$ cm$^{-2}$ with a corresponding sheet resistance of ~ 450 ohms/square. Ta/Ti/Al/Mo/Au source/drain, and Ni/Au gate contacts were placed in etched windows through the dielectric using CF$_4$, and SF$_6$/BCl$_3$/Ar RIE etches, respectively, defined by electron beam lithography.

DC and small-signal RF measurements were performed on dual-gate “U” configured devices with gate lengths ranging from 0.075 to 0.25 µm using coplanar waveguide probes contacting Ti/Au probe pads. The pinch off voltage for the Si$_y$N$_z$, and Al$_x$Si$_y$N$_z$ devices was -2.5 V and -1.5 V respectively, indicating that the barrier layers were recessed by the gate window etch. Both dielectrics yielded nominal reverse gate current on the order of 10 µA/mm at drain biases up to ~ 30 V, above which the gate current of the Al$_x$Si$_y$N$_z$ devices was lower than the Si$_y$N$_z$ devices. The $f_T$ was optimized at a gate length of 75 nm, and $f_{max}$ optimized at gate lengths of 200 nm, with maximum extrinsic values of 87 GHz and 150 GHz, respectively. The Al$_x$Si$_y$N$_z$-coated devices consistently had roughly 10% higher values of these device bandwidth metrics for the same gate footprint due to the reduction of key parasitic capacitances from a lower permittivity. The extracted source-gate resistance [3] showed a large non-linear dependence on drain current for the Si$_y$N$_z$ passivated devices. This effect is attributed to large longitudinal electric fields existing between the source-gate region [4]. Al$_x$Si$_y$N$_z$ devices, with reduced channel charge in the ungated regions show a source resistance nearly independent with drain current (Figure 2).

Large signal measurements were taken at 10 and 35 GHz. At 10 GHz, a series of power sweeps (optimized for PAE) were performed with drain biases ranging from 20 to 55 V (Figure 3). Maximum PAE measured 82% with 20 V on the drain, indicating that class-C operation was achieved on the harmonic load-pull bench used. At 40 V on the
drain the Al$_x$Si$_y$N$_z$ and Si$_y$N$_z$ devices yielded PAEs of 68% and 48% and output powers of 12.7 W/mm and 7.9 W/mm respectively (Figure 4). At 55 V on the drain the Si$_y$N$_z$ devices failed while the Al$_x$Si$_y$N$_z$ passivated devices yielded a PAE of 61% and a power density of 17.6 W/mm, which represents the highest performance values reported at 10 GHz for AlGaN/GaN HEMTs. At 35 GHz, the Al$_x$Si$_y$N$_z$ devices were tested (courtesy of Raytheon Integrated Defense Systems). They were matched for output power, and power sweeps were performed with drain biases ranging from 20 to 40 V. The devices had a maximum PAE of 35% at a drain bias of 20 V and a maximum output power density of 7.6 W/mm at a drain bias of 40 V.

References:

Figure 2: Source resistance as a function of drain current density. The Si$_y$N$_z$ devices suffer a large nonlinear increase in source resistance with drain current, while the Al$_x$Si$_y$N$_z$ devices are comparatively immune to this effect.
Fabrication of 3D Inter-Wafer Inductor with Magnetic Core

CNF Project # 1852-09
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Abstract:
One method of three dimensional (3D) power delivery architecture was proposed to vertically integrate a cellular array of voltage regulator modules (VRMs) on a thinned wafer with the microprocessor wafer using wafer-to-wafer bonding and through silicon vias (TSVs), with the inter-wafer inductor in between [1]. In this work, an inter-wafer inductor design with magnetic materials will be fabricated using 3D hyper-integration technology. Significant improvement on inductance and L/R ratio is the target of this work, comparing with air core spiral inductor in the frequency range of 1-200 MHz.

Summary of Research:
Power delivery is becoming a major issue in deep sub-micron microprocessors due to the rapid increase in power, clock frequency and the continuous decrease in the operation voltage [1]. As future technologies drive supply voltages lower, currents will be driven higher, and parasitics will become more and more problematic. Therefore, new solutions for power delivery are sought.

3D power delivery architecture would provide much shorter interconnects. This means, less parasitic, and significant improvements in the dynamic performance. In particular, it would provide multiple power supplies on the chip, suitable for multi-core processors, ASICs and 3D integrated circuits and systems.

Our group’s 3D power delivery architecture (see Figure 1) will vertically integrate a cellular array of VRMs on a thinned wafer with the microprocessor wafer using wafer-to-wafer bonding and TSVs, with the 3D inter-wafer inductor in between (see Figure 2). The magnetic core of the inductor will be fabricated in the CNF.

Reactive RF sputtering will be used as the method to fabricate the magnetic thin film. The target is made of CoFeAl. The sputtering gas is Ar and O₂. By varying the oxygen percentage in the gas, we could control the oxygen percentage in the thin film. The oxygen percentage is the key to have thin film with good soft-magnetic property and high resistivity.

RF sputtering for magnetic target is quite challenging, especially in the magnetron sputtering system. We managed to get the target sputtered by using very strong magnets (5000G) and thinning the target to 0.05 inch.

The preliminary results give us a good soft-magnetic thin film with a coercive force (Hc) as low as 15 Oe and an anisotropy field (Hk) as low as 100 Oe. The saturation field is as high as 2.3 kG. The resistivity is measured using a 4 point probe and is as high as 403μΩ*cm. Currently the thin film is a good soft-magnetic material. Further experiment will be done to reduce both the Hc and Hk, and increase the resistivity.

References:
Figure 1: One schematic of a 3D integration system.

Figure 2: Inductor designs consisting of Cu winding around a CoFeAlO core with (a) oval, (b) octagon, and (c) dodecagon geometries.

Figure 3: B-H graph of thin film $\text{Co}_{0.83}\text{Fe}_{2.25}\text{Al}_{1.93}\text{O}_{5.5}$. 
Abstract:
Suspended carbon nanotube transistors are used as nanoscale optoelectronic probes to investigate the electrical and optical processes in biological systems due to their high sensitivity, robust electrochemical stability, and high surface to volume ratio. Taking advantage of dual-optical trapping technique and scanning photocurrent microscopy, we are able to study the interface between carbon nanotubes and biomolecules such as DNA at the single-molecule level.

Research Summary:
Carbon nanotube-biomolecular hybrids have emerged as one of the most promising materials for biological and biomedical applications, such as biosensors, drug delivery, and imaging. Recently, carbon nanotubes (CNTs) have shown the ability to protect bound single-stranded deoxyribonucleic acid (ssDNA) cargos from enzymatic cleavage both during and after delivery into cells. This ability may result from the interaction between CNTs and ssDNA, which makes ssDNA unrecognizable to enzyme binding pockets. Furthermore, it is important to know whether ssDNA can be separated from CNTs in the presence of target complementary ssDNA. Therefore, we are interested in studying the interaction between CNTs and DNA.

Figure 1 shows the cross view of a CNT transistor. We etched a 7 µm wide and deep trench into a 170 µm thick fused silica substrate by the Oxford PlasmaLab 80+ RIE system. The source and drain electrodes (2 nm Ti, 40 nm Pt) were put beside the trench and separated by 9 µm. On the top of metal electrodes were the catalyst pads (10 nm of Al2O3, 0.2 nm of Fe) deposited by the evaporator.

Using a “fast heating” chemical vapor deposition method, we then grew the carbon nanotube which connects the source and drain. A 100 by 60 µm microfluidic poly(dimethylsiloxane) (PDMS) channel was sealed over the CNT, and a gold wire in a reservoir on the end of the channel was used to set the electrochemical potential of the solution [1].

Figure 2 illustrates the manipulation of DNA in our experiment. The ssDNA is attached to a microbead, which can be moved to different positions by optical trapping [2]. When the microbead is close to the CNT, the ssDNA forms a stable complex with individual CNTs by means of the aromatic interactions between nucleotide bases and CNT sidewalls (Figure 2, Left). After the ssDNA is attached to the CNT, we can separate them via the optical trap and directly measure the binding energy between them. If we label ssDNA, we can simultaneously study electrical transport and the fluorescence resonance energy transfer between CNTs and ssDNA. We can also introduce complementary ssDNA in the system, observe DNA hybridization process (Figure 2, Right) and study competitive binding of ssDNA with complementary ssDNA and ssDNA with CNTs. These experiments will not only extend the understanding of the interactions between DNA and CNTs, but also provide a new platform to probe in real-time and thus understand biomolecular interactions.

References:
Figure 1: Left, cross view of an electrolyte-gated suspended CNT transistor inside a PDMS microfluidic channel. Right, SEM image of a CNT suspended cross a trench and connected with two electrodes.

Figure 2: Left, schematic diagram of ssDNA wrapped around a suspended CNT transistor. Right, schematic diagram of a biological CNT sensor to detect DNA hybridization.