Abstract:
The performance of Al$_x$In$_{1-x}$N/GaN high-electron-mobility transistors (HEMTs) fabricated on silicon carbide (SiC) substrates is reported. Transconductance of 530 mS/mm with peak current density 1.4 A/mm is demonstrated. When driven at 10 GHz CW, output power of 4 W/mm with 43% PAE is observed.

Summary of Research:
Al$_x$Ga$_{1-x}$N/GaN high-electron-mobility transistors (HEMTs) are well-suited to high-frequency and high-power applications [1,2]. HEMT frequency scaling, by reducing the gate footprint, is not in itself sufficient to achieve high power performance at increasing frequency. The unity-current gain frequency is inversely proportional to the effective gate length,

$$f_T = \frac{v_{\text{eff}}}{(2\pi L_{\text{G,eff}})} \approx \frac{v_{\text{eff}}}{2\pi (L_{\text{G0}} + 2d)},$$

where $v_{\text{eff}}$ is the effective electron velocity in the gallium nitride (GaN) channel, $L_{\text{G}}$ is the gate length, and $d$ is the barrier thickness between the gate footprint and the two-dimensional electron gas (2DEG).

In order to maintain effective gate modulation and mitigate short channel effects, when reducing gate length, it is necessary to simultaneously reduce the barrier thickness [3]. To maintain a desirable current density, on the order of 1 A/mm, a thinned barrier dictates an increase in aluminum (Al) composition. Engineered high-Al composition Al$_x$In$_{1-x}$N barriers provide higher polarization induced sheet charge with lower strain than achievable using traditional Al$_x$Ga$_{1-x}$N barrier layers. In this work, the performance of Al$_x$In$_{1-x}$N/AlN/GaN-on-SiC HEMTs is investigated.

Al$_x$In$_{1-x}$N/AlN/GaN epitaxial layers were grown by metalorganic chemical vapor deposition (MOCVD) on 3" SiC substrates. The 1.85 µm GaN buffer was compensation doped with iron to increase its resistivity and mitigate subthreshold leakage current. The buffer was topped by a 15 Å AlN interbarrier and an 80 Å Al$_{0.85}$In$_{0.15}$N barrier.

The barrier composition was chosen to be Al-rich compared to lattice-matched Al$_{0.18}$In$_{0.82}$N/GaN case, thus leveraging piezoelectric polarization to further enhance the sheet charge density, $n_s$, of the 2DEG.

The surface morphology was characterized by atomic force microscopy (AFM). The 2DEG properties were examined by wetted Hg probe C-V, Lehighton, and transfer length method (TLM) measurements.

The devices were fabricated at the Cornell NanoScale Science and Technology Facility. A standard Ta/Ti/Al/Mo/Au ohmic contact recipe was used. Mesa isolation was achieved via a Cl$_2$/BCl$_3$/Ar ICP etch following the 800°C ohmic contact anneal. The wafer was passivated with 45 nm plasma enhanced chemical vapor deposition (PECVD) SiN$_x$ at 375°C, which was etched by CF$_4$ and field-plated, Γ-shaped Ni/Au gates were deposited.
TLM measurements were performed using the four-point probe technique. Direct current (DC) characterization and small-signal measurements were completed using on-wafer GSG probes. Power-matched large-signal measurements were made using a Maury load-pull system at 10 GHz CW.

AFM measurement of the Al_{1-x}In_{x}N surface indicates an RMS roughness of 0.6 nm for a 10 µm scan. The 2DEG density is measured by C-V at multiple sites on the wafer as \( n = 2.2 \times 10^{13} \text{ cm}^{-2} \). Excellent agreement is observed with a Schrödinger-Poisson model of the epitaxial layers. Lehighton measurements mapped across the 3″ wafer prior to processing indicate \( R_\text{sh} = 252.6 \pm 16.2 \Omega/\square \). This is in good agreement with TLM results for the SiN_{x}-passivated Al_{1-x}In_{x}N material, presented in Table 1 alongside data from a 20 nm-Al_{0.26}Ga_{0.74}N/GaN-on-SiC wafer, which was processed in parallel.

A study of anneal temperatures 740°C-820°C in 20°C increments confirms optimal contact formation at 800°C, which is used for the devices in this work.

Considering a representative 2 × 50 µm HEMT with \( L_{\text{GD}} = 1.5 \mu m \), peak DC metrics include \( I_{\text{D0}} = 1.03 \text{ A/mm} \), \( I_{\text{D1Vgs}} = 1.37 \text{ A/mm} \), and \( g_{\text{m}} = 530 \text{ mS/mm} \) (Figure 1).

For this device with a 0.15 µm field-plated gate footprint, the unit-current-gain frequency \( f_t = 37 \text{ GHz} \), and breakdown onsets at 37 \( V_{\text{DS}} \) and is preceded by an increase in gate current.

The SiN_{x} passivated devices exhibit ~20% drain lag in the knee region when driven with 500 ns pulses at a low duty cycle from \( V_{\text{OSQ}} = 20 \text{ V} \) and \( V_{\text{OSQ}} = -5 \text{ V} \). Inhibited by DC-RF dispersion and restricted by breakdown to 20 \( V_{\text{DS}} \) bias, output power in deep class AB operation driven at 10 GHz CW is 4.0 W/mm with 43% PAE.

Al_{1-x}In_{x}N/GaN epitaxial layers on a high-thermal conductivity substrate such as SiC are a promising platform for achieving efficient, high power, high frequency operation. The thinner barrier facilitates scaling device geometries well into the mm-wave regime.

Compared to typical Al_{x}Ga_{1-x}N/GaN device values, the relatively poor ohmic contact even at an optimized anneal temperature prompts a contact metallization study for high-Al composition, wider bandgap Al_{1-x}In_{x}N barriers. It is observed that channel breakdown is seeded by an increase in hot electrons tunneling through the sharp Al_{1-x}In_{x}N barrier; this motivates the \textit{in situ} growth of a GaN cap layer [4] or the deposition of a thin gate dielectric [5] to reduce the tunneling probability.

References:


<table>
<thead>
<tr>
<th>Al_{1-x}In_{x}N/AlN/GaN</th>
<th>Al_{x}Ga_{1-x}N/GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_e ) (Ω-mm)</td>
<td>0.62 ± 0.05</td>
</tr>
<tr>
<td>( R_{\text{sh}} ) (Ω/□)</td>
<td>250.3 ± 9.5</td>
</tr>
</tbody>
</table>

Table 1: Contact properties by four-point probe TLM.