A Process Technology for Fabricating Submicron Ballistic Electron Vertical Diodes for THz Frequency Power Generation

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Abstract:
GaN ballistic or quasi-ballistic electron devices require short transit distances in the order of a mean free path to avoid longitudinal optical phonon LO emission. Vertical current flow by design takes full advantage of the abrupt and thin layers grown by molecular beam epitaxy (MBE). Moreover, crystal orientation becomes important when ballistic transport is involved since bandstructure depends on direction and ballistic devices utilize the portions of the conduction band where parabolic assumption does not hold. C-axis growth of GaN is very mature and produces very high quality crystals and for ballistic devices with vertical current flow, this offers a unambiguous known bandstructure. In this summary, our process development efforts for a ballistic diode for terahertz (THz) generation based on negative differential conductivity is presented [1-3].

Summary of Research:
The process begins with the definition of the active mesa by a dry etch process (ICP) in chlorine based chemistry. A 100 nm thick carbon film was used as a hard mask due to its high selectivity with GaN and its inert nature. The carbon mask, due to its large grain size also needs patterning with another mask. The process sequence is:
1. Evaporate carbon on the chip without any mask.
2. Liftoff Cr using high resolution e-beam lithography.
3. Dry etch carbon in O$_2$ plasma masked by Cr.
4. Wet etch Cr to prevent it from sputtering in low pressure, high power chlorine based chemistry.

The lower level ohmic contact lift-off is done using e-beam lithography. Ohmic resistances are measured and recorded at this step. Then, a plasma enhanced chemical vapor deposition (PECVD) of 400-500 nm Si$_3$N$_4$ follows (higher than the mesa). This dielectric layer is deposited to be utilized in the planarization and passivation of the GaN surface.

Before the high temperature ohmic anneal, the whole chip is taken through a stepped anneal process in
order to out diffuse impurities and prevent cracking at high temperatures. This stepped anneal process is accomplished by executing a rapid thermal annealer (RTA) recipe which begins from 350°C and increments 50°C and stays there 30 seconds all the way up to 850°C. This way, it was observed that nitride cracking was prevented at high ohmic anneal temperatures. The presence of the Si$_3$N$_4$ film while annealing also helps prevent ohmic metals from creeping down the mesa edges and shorting the channel. Si$_3$N$_4$ coverage is very conformal as can be seen from the SEM image shown in Figure 3.

Shipley 1813 g-line photoresist is spun to a thickness much greater than the underlying topology to facilitate planarization of the surface. The mesas in the chip layout are intentionally distributed in the radial direction to minimize photoresist streaking during spinning. A specific RIE recipe is developed to yield 1:1 selectivity between Shipley 1813 photoresist and PECVD Si$_3$N$_4$ deposited at 400°C. Experiments were done specifically with small resist openings on witness nitride layers deposited on Si samples. Film thickness was continuously monitored using interferometry. The resist was not hardbaked to allow 1:1 selectivity.

The bulk of the photoresist is etched using O$_2$ plasma. The critical stage of the etch is done using the previously developed 1:1 selectivity recipe. This critical step is conducted in stages. At each stage, the thickness of the resist is monitored by interferometry. Final confirmation of the structure is obtained by atomic force microscope (AFM) as shown in Figure 4. Planarization is followed by SiO$_2$ deposition. SiO$_2$ is a low-κ dielectric and was chosen to minimize parasitic capacitances. Only the thinnest necessary layer of the high-κ Si$_3$N$_4$ seed layer was chosen to minimize the parasitic capacitances, while optimizing passivation of the GaN surface and maximizing heat removal from the GaN mesa. SiO$_2$ on top of the mesa is etched away for electrical access. It is achieved by first a dry etch then wet etch using diluted HF to have high selectivity between Si$_3$N$_4$ and SiO$_2$.

A separate etch step is necessary for both opening the extension of the cathode for ground pad metallization (for cascade probing) and top ohmic contact test patterns since Si$_3$N$_4$ thickness outside the device area is thicker as a result of photoresist planarization. Anode ohmic metallization is achieved with lift-off. A final layer of 400 nm gold evaporated to maximize heat spreading through the metal contacts and increase conductivity.

References:

Figure 3: Photoresist spun for planarization.

Figure 4: AFM image showing the tip of the mesa extending 120 nm out of the nitride opening for electrical contact. SEM shows incomplete etch step.