Study and Optimization of a Process for Activating Backside Junctions on Thin Silicon Pixel Detectors for High Energy Physics

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Abstract:
This project is part of a larger effort to develop thinned (~ 50 µm) silicon pixel detectors for particle detection in high energy physics experiments. These detector arrays will contain active CMOS pixel circuitry on the top of the wafer and require formation of an extremely low leakage backside junction at the end of processing. Static temperatures must remain below 450°C during the processing to protect the sensitive frontside circuitry. Pulsed laser annealing is currently the most promising method for achieving suitable activation of this backside implant. This project focuses specifically on understanding and optimizing a process for activating backside junctions, initially on conventional wafers and ultimately proving the process on thinned substrates. We performed initial work using planar diodes fabricated on conventional wafers for optimization of the diode reverse leakage properties.

Summary of Research:
A range of diodes, with guard rings, was fabricated at the CNF, areas ranging from 0.01 mm² to 400 mm² (see Figure 1, left, for layout).
Leakage current scaling with both area and perimeter was determined.
Conventional p-n junctions were fabricated on standard 100 mm p-type wafers. The following processing steps were performed:
- Thermal oxidation as implant mask
- Photolithography for implant mask
- Implant at Core Systems, 1x10¹⁵ P at 125 KeV
- Blanket laser annealing in Prof. Thompson’s lab
- PECVD for contact vias
- Photolithography of contact vias
- Aluminum metallization
- Metal photolithography and etch
- Device test: IV curves using Keithley Probe Station

Figure 2, left: A cross-section of the device. Initial device tests revealed leakage currents on the order of 10⁻⁴ A. These initial results will require follow-up work to optimize fabrication, implantation and laser anneal parameters to reduce the leakage current.