Fabrication of AlGaN/GaN High Electron Mobility Transistors (HEMTs) with High-Temperature Dielectric Passivations

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Abstract:
AlGaN/GaN high electron mobility transistors (HEMTs) utilize dielectric passivations to tie up surface states that can trap charge during device operation. Traditionally, a low-temperature Si$_y$N$_z$ dielectric is deposited on the device after the placement of source, drain and gate to passivate the exposed AlGaN. In this study, we explore the use of high-temperature passivations consisting of Si$_y$N$_z$ and Al$_x$Si$_y$N$_z$. High-temperature passivations are superior in film quality to low-temperature films, but introduce difficulty in the fabrication process since they must be deposited prior to any metal deposition to avoid degrading the metal.

Summary:
The AlGaN/GaN HEMTs in this study consist of a thin (~ 25 nm) AlGaN layer epitaxially grown on a thick GaN layer (~ 1 µm) on a SiC substrate. A 2-dimensional electron gas (2DEG) forms at the AlGaN/GaN interface due largely to the electric fields arising from difference in the spontaneous polarizations of the GaN and AlGaN crystal lattices, with a smaller contribution from the piezoelectric strain in the pseudomorphic AlGaN layer [1]. This 2DEG forms the conduction channel of the transistor. Due to the thinness of AlGaN layer, the device is very sensitive to surface charges and requires a passivation to stabilize the surface states which can trap charges and deplete the 2DEG forming the conduction channel leading to dispersive behavior during device operation at high frequencies.

Fabrication of the device begins with an epitaxial growth of the AlGaN/GaN layers via molecular beam epitaxy on SiC substrates. The active areas are defined and electrically isolated by i-line lithography and subsequent inductively coupled plasma / reactive ion etching (ICP/RIE). This also forms etched alignment marks to be used for both optical and electron beam lithography.

The mesas are then coated in a modified low pressure chemical vapor deposition (LPCVD) system with Si$_y$N$_z$ and Al$_x$Si$_y$N$_z$ at 750°C. The ability to incorporate Al into the Si$_y$N$_z$ film was made possible by the addition of an organometallic Al source to a commercial LPCVD system equipped with dichlorosilane and ammonia precursors.

The gate notch is patterned with either electron beam or optical lithography and is etched into the dielectric with a CF$_4$ RIE etch or a low-bias SF$_6$/BCl$_3$/Ar ICP/RIE etch. The AlGaN may optionally be recessed in the gate notch for enhanced performance with a low-bias BCl$_3$/Ar ICP/RIE etch. Figure 1 shows that the low-bias etch is most likely beneficial, as capacitance voltage measurements of the 2DEG density on a bare sample show the CF$_4$ etch is very damaging to the surface while the low-bias one is not.

Ohmic contacts are defined in a bilayer of resist with a reentrant profile using electron beam or optical lithography and the dielectric is etched with CF$_4$ plasma. This is followed by a SiCl$_4$ RIE pretreatment step prior to a Mo/Al/Mo/Au metalization and 500°C rapid thermal anneal (RTA). The pretreatment step has been found to give low-resistance ohmic contacts with an anneal temperature below the melting point of any of the metals used [2]. Annealing at a temperature below the melting point of the metals used yields superior edge roughness than traditional schemes which use metals that require...
high temperature anneals. As noted in Figure 2 the annealed metal has a smooth morphology. The anneal step also serves to recover any damage to the gate notch region induced by the etching.

The gate metalization is defined with either electron beam or optical lithography in a resist bilayer with a reentrant profile and a Schottky contact consisting of a thick Ni/Au stack is then lifted off. Finally thick Ti/Au pads are lift off to provide electrically probable connections to the device.

Devices have been fabricated with the above process, however the ohmic contact step has been problematic. Experiments have shown that using the same resist stack (either photoresist or electron beam resist on top of the LOR series of lift off resists) to perform the etch and pretreat as well as the metal lift off yields low resistance ohmic contacts post anneal. However it leaves behind a residue from the lift off resist layer that cannot be removed. This residue is formed by a reaction of the LOR resist with the SiCl$_4$, and it interferes with the placement of the gate metalization. Devices have been fabricated with optical lithography that place the gate far enough away from the residue that it does not interfere with the operation of the device, however this introduces large parasitic resistances which degrade device performance. Ge is currently being investigated as a candidate to replace the LOR layer as it would serve the same function and is easily removed. This would allow for a single lithography step to define the ohmic contacts as Ge does not react with the SiCl$_4$.

Development is ongoing to create a process where source, gate and drain regions are all defined by electron beam lithography so as to allow for small gate footprints with tight alignment tolerances to the source and drain.

References: