Abstract:

We report the fabrication process, material and electrical characterizations of ultra thin body (UTB) thin film transistors (TFTs) by using in situ doped polysilicon followed by the chemical mechanical polishing (CMP) process. The resulting polysilicon film is about 13 nm thick with approximately $10^{19}$ cm$^{-3}$ body doping. Root mean square (RMS) surface roughness below 1 nm is achieved over 25 µm$^2$ area, tested by atomic force microscopy (AFM). The number density and average diameter of nanocrystals (NCs) embedded in a dielectric layer of the UTB TFT are $7.5 \times 10^{11}$ cm$^{-2}$ and 6.1 nm, respectively. Furthermore, scanning transmission electron microscopy (STEM) is performed for material characterization. We obtain a memory window of about 3.8V by ±6V program/erase (P/E) voltages. Therefore, UTB TFT becomes a promising candidate for the three dimensional (3D) integration in high-density nonvolatile memories.

Summary:

High-density nonvolatile memory applications can benefit tremendously from three-dimensional (3D) integration with low power consumption. Among several proposals [1-4], the planar polysilicon thin-film transistor (TFT) with metal nanocrystals (NCs) and high-k gate-stack is one of the promising candidates. Metal NCs were introduced to allow thin tunnel dielectric, lower the program/erase (P/E) voltage and enhance the cycle endurance [5]. One of the key device designs is to achieve a uniform ultra-thin-body channel region without implant dopant activation, where the threshold voltage $V_{th}$ is less affected by traps in the polysilicon grain boundaries due to the reduced volume to be depleted before inversion [6,7]. Moreover, reduced surface roughness by full-wafer chemical mechanical polishing (CMP) [8] leads to improved device characteristics and reliable process integration.

The device structure under study is shown in Figure 1. A 100 nm thick polysilicon film with $10^{19}$ cm$^{-3}$ in situ phosphorous doping was deposited on 200 nm PECVD oxide. Surface morphology of deposited film by AFM is shown in Figure 2(a), which gives a root mean square (RMS) roughness of about
3.5 nm. CMP was then applied to achieve the desired film thickness of 13 nm with RMS roughness below 1 nm as shown in Figure 2(b). This is an important step since rough surface affects P/E consistency by nonuniform vertical fields [9], increases the interface states that degrades the cycle endurance, and reduces the transconductance due to the additional surface scattering.

After CMP, an Al2O3 film with equivalent oxide thickness (EOT) of 2.6 nm and physical thickness of 6 nm was grown as tunnel dielectric by atomic layer deposition (ALD). A process split of sputtered (Ti,Dy)Ox as tunnel dielectric with the same EOT and physical thickness of 23 nm was also executed. Au NCs was self-assembled on tunnel dielectric by e-beam evaporation [10].

The (Ti,Dy)Ox film as control dielectric was deposited by sputtering with EOT of 4.5 nm and physical thickness of 40 nm. Finally, the 50 nm Cr gate electrode was deposited by e-beam evaporation. After gate patterning, the device was annealed in the forming gas (H2:5%) at 400°C for one hour.

Figure 3(a) shows the lack of memory windows in the control devices with the same gate stack but without Au NCs. The off-state leakage current is at $6 \times 10^{-12}$ A/µm for $V_{DS} = 0.5$V and $V_{GS} = -0.5$V. The output characteristics of the Al2O3/Au/(Ti,Dy)Ox device were shown in Figure 3(b). The kink effect was eliminated due to extremely flat ultra-thin film in comparison with the conventional TFT.

Figure 4(a) shows reasonable subthreshold slopes (S) and memory windows of the Al2O3/Au/(Ti,Dy)Ox device for various gate voltage sweeps. We have obtained a memory window of about 3.8V by ± 6V P/E voltages. Retention characteristics were monitored in the Al2O3/Au/(Ti,Dy)Ox and (Ti,Dy)Ox / Au/(Ti,Dy)Ox devices after writing by ± 6V direct pulse of 1 sec duration in Figure 4(b). The much longer retention time and much larger memory window in the Al2O3/Au/(Ti,Dy)Ox device is attributed to the 3D electrostatics when the dielectric constant of control dielectric is much larger than that of the tunneling dielectric [5].

Carrier transport was confirmed to be Frenkle-Poole emission in sputtered (Ti,Dy)xOy and direct tunneling in ALD Al2O3 due to the different trap densities, which also helps the retention time in the Al2O3/Au/(Ti,Dy)Ox.

In conclusion, we have demonstrated a low-temperature TFT process for 3D nonvolatile memory integration.

References: