Polysilicon-on-Insulator Photonic Devices

CNF Project # 980-01
Principal Investigator: Prof. Michal Lipson
Users: Kyle Preston, Brad Schmidt, Po Dong

Affiliation: School of Electrical and Computer Engineering, Cornell University
Primary Funding: NSF, Intel Corporation
Contact: lipson@ece.cornell.edu, kjp32@cornell.edu
Web Site: http://nanophotonics.ece.cornell.edu

Abstract

Integrated optical interconnects based on silicon photonic devices appear promising to replace metallic interconnects, which increasingly are the limiting factor in high-performance microelectronics. Most of the major advances in silicon photonics have been based on single-crystalline silicon-on-insulator (SOI), whose material properties are well-understood due to extensive investment by the microelectronics industry. However, large-scale integration of photonics and microelectronics will require multiple vertical layers of electrically-active material. We demonstrate optical microresonators in complementary metal oxide semiconductor (CMOS)-compatible polycrystalline silicon with intrinsic quality factors of 20,000. The resonators can be coupled in-plane to polysilicon waveguides, or coupled vertically to low-loss crystalline silicon waveguides for dense integration on chip.

Summary of Research

Polycrystalline silicon may be a flexible solution for rapid integration and immediate introduction of active photonics into standard CMOS chips [1]. Due to its relatively poor optical properties, polysilicon has largely been ignored by the photonics community, with a few notable exceptions: a three-dimensional photonic crystal with a band gap at infrared wavelengths demonstrated by Lin et al. [2], passive all-polysilicon ring resonators demonstrated by Maki et al. [3], and a MOS-based electro-optic modulator by Liu et al. [4], which included a polysilicon gate built into a crystalline silicon waveguide. If low-loss waveguides (e.g., using amorphous silicon, crystalline silicon, or silicon nitride) could be utilized to efficiently guide light to and from resonant polysilicon devices, then the quality factor $Q$ of polysilicon resonators becomes our main figure of merit instead of total losses. Loaded $Q$ factors of 10,000 are achievable even with high optical losses of 35 dB/cm, and $Q$ values around 5,000-10,000 are sufficient to build state-of-the-art active devices such as electro-optic modulators [5].

To fabricate optical devices in polysilicon, a 2 μm silicon dioxide layer is thermally grown on a 4-inch silicon substrate and a 250 nm thin film of amorphous silicon is deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. The r.m.s. surface roughness of this film is measured by atomic force microscopy (AFM) to be ~0.3 nm. The sample is annealed in $N_2$ at 600°C and 1100°C.

The initial 600°C anneal crystallizes the sample into polycrystalline silicon, while the additional 1100°C anneal serves to maximize the crystallized fraction and remove defects from the crystalline regions [6]. The final r.m.s. surface roughness of the film is measured by AFM to be ~0.7 nm.

From this point on, the samples are treated just like commercial SOI wafers. E-beam resist is spun on and patterned by e-beam lithography, and the pattern is transferred by reactive ion etching using a standard
chlorine-based shallow silicon etch recipe. SiO$_2$ cladding is deposited by plasma-enhanced chemical vapor deposition (PECVD). An example polysilicon ring resonator laterally-coupled to a polysilicon bus waveguide is shown in Figure 1. The spectrum of this device is shown in Figure 2, with loaded $Q$ values over 10,000, intrinsic $Q$ values around 20,000, and high extinction ratios over 15 dB. To our knowledge, these are the highest values of $Q$ demonstrated in polysilicon optical resonators.

We have also shown loaded $Q$ values of 4,000 in polysilicon films annealed at only 600°C, demonstrating the range of $Q$ values that can be obtained with different thermal budgets.

Additionally, we show polysilicon ring resonators vertically coupled to low-loss crystalline silicon waveguides. We start with a commercial SOI wafer containing a 3 µm buried oxide (BOX) layer and a 250 nm-thick silicon layer. Waveguides are patterned in the crystalline silicon layer by e-beam lithography and reactive ion etching, and a 350 nm film of oxide is deposited by PECVD from a tetraethoxysilane (TEOS) precursor. Then the fabrication steps of the previous paragraph are repeated on the new substrate to build polysilicon resonators. Figure 3 shows an SEM of a polysilicon ring resonator and a buried silicon waveguide before the final oxide cladding. Figure 4 shows a spectrum of such a device with loaded $Q$ values over 4,000.

To our knowledge, this is the first demonstration of this type of mixed-silicon optical system.

References


