Tera-Bit Metal Nanocrystal Nonvolatile Memories and Interfaces

CNF Project # 715-98
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Abstract
To realize nonvolatile information storage at the tera-bit scale, we have explored several promising approaches such as metal nanocrystal memory and molecular memory with mono-dispersed fullerenes. Besides its potential high bit-density, metal nanocrystal memory has the unique opportunity to achieve low program/erase voltage with robust reliability, which is otherwise not possible in the current Flash or SONOS technology. Moreover, our study of the fullerene-embedded memory also shed light on a feasible molecular interface with complementary metal oxide semiconductor (CMOS) circuits through a floating gate implementation.

Summary
A fast and reliable nonvolatile memory is an essential component of an information processing system and our research group is pursuing several promising approaches in this area. Previously we have demonstrated the feasibility of metal nanocrystal memory to lower the program/erase (P/E) voltage, improve cell density, and reduce P/E time while keeping retention time and endurance to the specifications used currently [1]. We have now built trustworthy models to understand the design space [2-3], using experimental data obtained with both MOS and carbon nanotube (CNT) channels [4] to calibrate the transport parameters such as effective mass and tunneling cross sections. With optimization strategies in both nanocrystal arrays and the heterogeneous gate stack, a metal nanocrystal memory design with 1.0 V memory window, 13 µs programming, 2.5 µs erasing and over 10-year retention time has been demonstrated at ± 4 V operation (Figure 1), which highlights the potential of nanocrystal memories as the next-generation nonvolatile memory.

In the course of this work we have also found that opposite polarities of charge storage happened in Au metal NC memories with different control oxides (Figure 2). The effective NC work function is found not only a bulk property of the NC, but also governed by the interface.

Figure 1: The calculated program, erase, and retention characteristics of a scaled NC memory design operated at ± 4 V.

Figure 2: CV measurements of Au metal NC capacitors with Al₂O₃ control oxide and evaporated/PECVD SiO₂ control oxide.
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with surrounding dielectric, as a result of the Fermi-level pinning [5]. This fundamental interface property should be taken into account in the selection of NC and dielectric materials for the NC memory optimization.

Driven by the ever increasing need for high density digital memory at low cost, we also have demonstrated the possibility of using carbon molecules in the form of fullerenes (C\textsubscript{60}), also known as “bucky balls,” as an electrostatic non-volatile memory storage device [6]. We can employ C\textsubscript{60} nonvolatile memory cells to experimentally program four C\textsubscript{60} molecular orbital states, C\textsubscript{60}\textsuperscript{0}, C\textsubscript{60}\textsuperscript{1}, C\textsubscript{60}\textsuperscript{2}, and C\textsubscript{60}\textsuperscript{3} (Figure 3). This was possible because the mono-disperse nature and molecular size of C\textsubscript{60} results in a very sharp Coulomb staircase that can be observed at room temperature. A physical model based on the molecular orbit structure, the 3-D electrostatic charging energy, and the Fermi-level pinning theory yields good quantitative agreement with experiments. This result not only leads to a better understanding of the C\textsubscript{60} molecular orbital structure and corresponding chemical redox levels, but could also potentially pave the way for realizing reliable multi-level molecular memories. Furthermore, this is the first demonstration that the CMOS circuit system can directly control and sense the redox states of nano-scale molecules.

References


