Gallium Nitride Ballistic Electron Acceleration Negative-Differential-Conductivity Diodes for Terahertz Applications

CNF Project # 370-89
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Abstract
Electronic generation of terahertz (THz) signals using gallium nitride (GaN) is predicted to exhibit high efficiency. Theory by Ridley et al. [1] shows that electrons in an ultra thin (20-120 nm) epilayer of intrinsic GaN can be ballistically accelerated to negative mass states (under the influence of an applied bias voltage of 2.7 volts) with hot enough injection. If a majority of the electrons can be made to populate these states, negative-differential-conductivity (NDC) will be observed at the device terminals.

Summary of Research
Both GaN n*-i-n* structures and structures with aluminum gallium nitride (AlGaN)/GaN launchers (for 0.38 eV injection) have been fabricated and characterized. However, no negative differential conductivity has been observed yet, mainly due to parasitics and related heating problems (Figure 1).

The heating problem is mainly a direct consequence of high operating current densities in the order of 1-2 MA/cm². These high current densities combined with finite parasitic resistances (i) causing permanent damage to contacts through catastrophic IR heating (ii) and causing a voltage drop across the i-layer diameter due to spreading resistance, which introduces field non-uniformity. If this voltage drop is too high, it will suppress the NDC effect. The fact that hot ballistic electrons dump their kinetic energy into the N⁺ region near the contact also contributes to the heating problem mentioned above.

These problems in our new design are addressed through a thicker intrinsic region which will reduce the current densities by a factor of sixteen while maintaining the ballistic nature of the transport, and our expectations are strongly supported by Wraback’s experiments [2, 3] which clearly show NDC at electric fields even below (electron transfer) threshold voltages at distances up to a quarter micron.

Figure 1: IV curves for a 5 µm diameter 30 nm i-layer diode (pulsed vs. continuous wave bias regimes).

Figure 2: New geometry vs. old geometry.
One other geometry to overcome the parasitics and heating issues has been designed and planned but not fabricated yet (Figure 2). In this design, the active region is 1 µm in diameter whereas the contact area is 25 times larger. This is accomplished by etching a conic shaped mesa using ion milling techniques. Concentrating the current in 1 µm diameter will help reduce the spreading resistance. In addition, a 25 times greater area will reduce the I2R heating at the contact which results in catastrophic failure. However there are high frequency performance concerns about this design due to the 2 µm mesa height it requires from the processing point of view and the relatively thin skin depths at those frequencies.

GaN epilayers for this research are grown on N⁺ SiC substrates in our own MBE lab. We process 15 mm² samples. First we dry etch the cylindrical mesas using the ICP tool reserved for III-V’s. Then we evaporate the ohmic contacts followed by the oxide deposition. To make contacts to the devices, the oxide is drilled first (with sloped walls for continuous metal coverage), and is followed by an electroplating process which lays out the probe pads in electrical contact with the device.

References


C-Doped Semi-Insulating GaN HFETs on Sapphire Substrates with a High Breakdown Voltage and Low Specific On-Resistance

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Abstract

High breakdown voltage (BV) aluminum gallium nitride/gallium nitride (AlGaN/GaN) heterojunction field effect transistors (HFETs) with a low specific on-resistance ($AR_{DS(on)}$) were successfully fabricated using intentionally C-doped semi-insulating GaN buffers with a high resistivity on sapphire substrates. A high BV of ~1600 V and low $AR_{DS(on)}$ of 3.9 mΩcm$^2$ was achieved from the fabricated devices with no field plate design. This result is almost touching the 4H-SiC theoretical limit and is a record achievement for GaN HFETs realized on sapphire substrates, to the best of our knowledge. Additionally, the effects of gate-drain spacing ($L_{gd}$) on device characteristics were investigated through device fabrication and characterization.

Summary of Research

Figure 1 illustrates the schematic cross-sectional structure of fabricated AlGaN/GaN HFETs with a C-doped semi-insulating GaN buffer on sapphire substrates. The GaN-based heterostructures were based on GaN grown by metal-organic chemical vapor deposition on c-plane sapphire substrates, given its cheaper price and larger wafer size than SiC substrates. The fabrication began with evaporated Ti/Al/Mo/Au (15/90/45/55 nm) for the source/drain ohmic contacts. The devices were annealed at 800°C for 30 s under N$_2$ ambient in a rapid thermal annealing (RTA) system. Next, the mesa isolation was performed by reactive ion etching with chlorine-based gas mixture (Cl$_2$/BCl$_3$/Ar). From on-wafer transfer-length measurements, an ohmic-contact transfer resistance of 0.5 Ω-mm and a sheet resistance of 540 Ω/□ were obtained. Thereafter, a 600 nm thick oxide insulation layer was deposited on the mesa-etched region to eliminate pad-to-pad leakage current paths and then was wet-etched. The Ni/Au (50/300 nm) gates were evaporated and lifted off. Finally, a 60 nm thick SiN was deposited at a substrate temperature of 300°C using plasma-enhanced chemical vapor deposition. A
surface heat treatment (500°C/10 min) under N₂ ambient in the RTA system was performed for surface stabilization, immediately before the SiN deposition. Fabricated devices with source-gate spacing ($L_{sg}$) of 2 µm, gate length ($L_g$) of 2 µm, gate width ($W_g$) of 250 x 2 µm and $L_{gd}$ of 5, 10 and 16 µm were prepared, and $L_s$ and $L_d$ were both varied from 7 to 40 µm to optimize device performance.

Figure 2 presents the on-state $I_{DS}$–$V_{DS}$ characteristics of the fabricated devices. The devices showed excellent pinch-off characteristics and maximum drain current density ($J_{DS, max}$) for $L_{gd} = 5, 10$ and 16 µm were 460, 410 and 360 mA/mm under the gate-source voltage ($V_{GS}$) of 1 V, respectively. It was also observed that $L_{gd}$ has a strong effect on $AR_{DS(ON)}$. Here, the device active area was defined by the mesa isolation process. The $AR_{DS(ON)}$ increased almost linearly with increasing $L_{gd}$, and the measured $AR_{DS(ON)}$ values of $L_{gd} = 5, 10$ and 16 µm were 1.6, 2.4 and 3.9 mΩcm², respectively.

Figure 3 shows the off-state breakdown characteristics of the fabricated AlGaN/GaN HFETs. Here, all of the breakdown characteristics were observed under $V_{GS}$ of −5.5 V and fluorinert FC-40 was applied on the surface of the fabricated devices for BV measurements to avoid problems with arcing and tracking due to environmental conditions [1]. A high BV over 1560 V was achieved on the fabricated HFETs with $L_{gd} = 16$ µm. At this length of $L_{gd}$, the average breakdown field along the channel was only 1 MV/cm, compared with the ideal GaN breakdown strength of 3 MV/cm. This means that the peak electric field is near the gate edge, and gives room for further material and process development. Furthermore, burnout marks were found on the surface of the device active area after destructive BV measurements. For $L_{gd} = 5$ µm, burnout marks were clearly found between gate and drain. On the other hand, burnout marks for $L_{gd} = 16$ µm were in the whole active area due to a relatively high applied bias between drain and source. However, the measured BVs increased clearly with $L_{gd}$ and were 400, 770 and 1560 V for $L_{gd} = 5, 10$ and 16 µm respectively. It is suggested that the actual device breakdown was determined by the gate-drain breakdown, yielding BVs increased with $L_{gd}$.

Figure 4 presents the BV–$AR_{DS(ON)}$ relations for the fabricated devices with $L_{gd}$ of 5, 10 and 16 µm. The trend of BV–$AR_{DS(ON)}$ showed a clearly linear relation in the log-log plot, suggesting that the device performance is very predictable with the variation of $L_{gd}$. It was also shown that the results of this work were very reproducible, when compared with our previously published results [2, 3]. In particular, a BV over 1560 V and $AR_{DS(ON)}$ of 3.9 mΩcm² was accomplished from the fabricated GaN-based HFETs realized on sapphire substrates and this result is even touching the 4H-SiC theoretical limit.

References


Figure 3: Off-state breakdown characteristics of the fabricated AlGaN/GaN HFETs.

Figure 4: Relations between $AR_{DS(ON)}$ and BV for References [9, 10] and this work.
AlGaN/GaN High-Electron-Mobility Transistors on Different Substrates

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Abstract
The performance of aluminum gallium nitride/gallium nitride (AlGaN/GaN) high-electron-mobility transistors (HEMTs) on diamond and silicon carbide (SiC) substrates is examined. Additionally, the temperature rise in similar devices on diamond and SiC substrates is reported. Recently, identical AlGaN/GaN HEMTs have been fabricated at Cornell NanoScale Science & Technology Facility (CNF) on diamond, bulk GaN, and SiC substrates.

Introduction
AlGaN/GaN HEMTs are well-suited to high-frequency and high-power applications [1, 2]. SiC is presently the substrate of choice for high-performance GaN HEMTs with a thermal conductivity an order of magnitude greater than that of sapphire. Bulk GaN is of interest as a substrate for the low dislocation densities in the epitaxial layer and an expectation of improved reliability. However, regardless of substrate, thermal limitations on device performance emerge under conditions of high bias and power drive [3]. Electron mobility has been observed to decrease in AlGaN/GaN HEMTs as a function of temperature rise, \( \mu \sim T^{-1.8} \) [4]. This decrease induces an increase in knee voltage which limits the dynamic range of large-signal operation.

Further advancement of GaN HEMTs for high-power applications requires reducing the temperature rise of the devices; the solution reported in this paper involves locating the device structure within close proximity to CVD diamond, which has a thermal conductivity 3-4 times that of SiC [5]. Group4 Labs has developed a method to atomically attach GaN epitaxial layers to polycrystalline diamond [5]. As previously reported [6] and supported by our results, the attachment process leaves the two-dimensional electron gas (2DEG) confinement layer intact.

Comparative experimental study of the HEMT operating temperature rise requires a localized technique. Scanning thermal microscopy involves the replacement of the AFM tip with a microscopic resistive filament, which acts as one leg of a Wheatstone bridge. Operating temperature measurements have been completed as a function of dissipated power density, in W/mm, on diamond and SiC substrates.

Summary of Research
The GaN-on-diamond material was prepared by Group4 Labs [5]. Material on GaN and SiC substrates was grown by General Electric and Northrop Grumman, respectively. The devices were fabricated at the CNF. The HEMTs on diamond substrate were fabricated exclusively via electron beam lithography, necessitated by bowing on the order of 50 \( \mu \text{m} \) over 1 cm

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. To ease handling, the GaN-on-diamond wafer was mounted to a 15 mm x 15 mm carrier using Crystalbond 509 adhesive and dismounted before each processing step that exceeded 170°C temperature.

A standard Ti/Al/Mo/Au ohmic recipe was used, including a post-deposition anneal. Mesa isolation was achieved after ohmic contact anneal via an inductively coupled plasma (ICP) Cl

2/BCl

3/Ar etch. Finally, the devices were passivated with ~ 85 nm SiN deposited by plasma enhanced chemical vapor deposition (PECVD) at 375°C.

Transfer length method (TLM) measurements were performed via a four-probe technique using a Keithley 236 source measure unit (SMU). DC characterization was performed using an HP 4142 (Figure 1) and small-signal measurements were completed with an HP 8510 using Cascade on-wafer probes. Large-signal, class B, continuous-wave measurements were made using a Focus load-pull system powered by a traveling wave tube at 10 GHz (Figure 2).

Thermal measurements were performed on the HEMTs using a ThermoMicroscopes AFM-based SThM system with a DC drain-source bias applied across one channel of the device. The 5 \( \mu \text{m} \)-diameter platinum (or Pt/10%Rh alloy) filament was connected to the Wollaston wire.
cantilever arms. The probe tip was positioned in contact with the insulating SiN\textsubscript{x} layer atop the channel between the gate and drain. The finite temperature gradient in the SiN\textsubscript{x} is comparable for the devices on either substrate, as the passivation layers are the same thickness and were deposited at the same temperature. The thermal resistance of the devices on SiC was observed to be ~ 12°C/(W/mm), whereas using diamond substrate it was observed to be ~ 6°C/(W/mm) (Figure 3).

Ongoing work involves the characterization of identical devices on diamond, bulk GaN, and SiC substrates which have been processed at CNF.

References


Flat Panel Displays

CNF Project # 470-93
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Abstract

This project is concerned with glass substrates for flat panel display and electronics-on-glass applications. Photolithography and electron beam lithography were used to fabricate simulated particles on substrates down to 0.2 microns, which were then used to characterize metrology tools and to observe the effect of particles on film deposition processes. Exploratory work was also conducted in microfluidics for cell culture.

Summary of Research

This project is concerned with glass substrates for flat panel display and electronics-on-glass applications. As the design rules for devices in these technologies grow smaller, the sensitivity to particles of deposition and lithography processes on the substrates increases. Over the past year we have used the facilities of the Cornell NanoScale Science & Technology Facility to fabricate simulated particles on our substrates. Contact photolithography was used to replicate SiO$_2$ cylinders with diameters greater than two micrometers, and electron beam exposure of spin-on-glass in the JEOL 9300 was used for patterns with diameters down to 0.2 µm. These were then used to characterize metrology tools and to observe the effect of particles on film deposition processes.

Automated detection and measurement of particles on glass was found to be substantially more difficult than similar measurements on silicon. Developing methods for characterization of particles on glass substrates is an important topic, as coating studies show that the area of effect on film thickness and adhesion can be much larger than the initial particle size.

Future plans for this project include studying wet cleaning processes for glass substrates, followed by deposition of SiO$_2$ and Si$_3$N$_4$ thin films by both plasma enhanced chemical vapor deposition (PECVD) and low pressure chemical vapor deposition (LPCVD). These processes would help us to understand the coating influences on glass substrates with different compositions, as well as particle sensitivity. We will use this knowledge to continue developing novel thin film coatings on display substrates. It is believed that the processes we are developing at the CNF will enable the demonstration of new product concepts, and this technology will then be transferred to production.

Exploratory work was also conducted in microfluidics to study cells under a dynamic culture microenvironment in vitro. These approaches are being explored to study the effect of conditions on cell culture response and to better understand how cells respond to their microenvironment, in support of Corning Life Sciences. Microfluidic devices were fabricated from highly gas-permeable polydimethylsiloxane material by means of soft lithography. Standard photolithography methods were used to fabricate features in 10-500 micrometer range.
Figure 1: 5 µm simulated particle fabricated in SiO₂ on a display glass substrate.

Figure 2: 5 µm feature coated with 500 nm of silicon resulting in local delamination.
**Tera-Bit Metal Nanocrystal Nonvolatile Memories and Interfaces**

CNF Project # 715-98  
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**Abstract**

To realize nonvolatile information storage at the tera-bit scale, we have explored several promising approaches such as metal nanocrystal memory and molecular memory with mono-dispersed fullerenes. Besides its potential high bit-density, metal nanocrystal memory has the unique opportunity to achieve low program/erase voltage with robust reliability, which is otherwise not possible in the current Flash or SONOS technology. Moreover, our study of the fullerene-embedded memory also shed light on a feasible molecular interface with complementary metal oxide semiconductor (CMOS) circuits through a floating gate implementation.

**Summary**

A fast and reliable nonvolatile memory is an essential component of an information processing system and our research group is pursuing several promising approaches in this area. Previously we have demonstrated the feasibility of metal nanocrystal memory to lower the program/erase (P/E) voltage, improve cell density, and reduce P/E time while keeping retention time and endurance to the specifications used currently [1]. We have now built trustworthy models to understand the design space [2-3], using experimental data obtained with both MOS and carbon nanotube (CNT) channels [4] to calibrate the transport parameters such as effective mass and tunneling cross sections. With optimization strategies in both nanocrystal arrays and the heterogeneous gate stack, a metal nanocrystal memory design with 1.0 V memory window, 13 µs programming, 2.5 µs erasing and over 10-year retention time has been demonstrated at ± 4 V operation (Figure 1), which highlights the potential of nanocrystal memories as the next-generation nonvolatile memory.

In the course of this work we have also found that opposite polarities of charge storage happened in Au metal NC memories with different control oxides (Figure 2). The effective NC work function is found not only a bulk property of the NC, but also governed by the interface between the NC and control oxide.

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**Figure 1:** The calculated program, erase, and retention characteristics of a scaled NC memory design operated at ± 4 V.

**Figure 2:** CV measurements of Au metal NC capacitors with Al₂O₃ control oxide and evaporated/PECVD SiO₂ control oxide.
with surrounding dielectric, as a result of the Fermi-level pinning [5]. This fundamental interface property should be taken into account in the selection of NC and dielectric materials for the NC memory optimization.

Driven by the ever increasing need for high density digital memory at low cost, we also have demonstrated the possibility of using carbon molecules in the form of fullerenes (C\textsubscript{60}), also known as “bucky balls,” as an electrostatic non-volatile memory storage device [6]. We can employ C\textsubscript{60} nonvolatile memory cells to experimentally program four C\textsubscript{60} molecular orbital states, C\textsubscript{60}\textsuperscript{0}, C\textsubscript{60}\textsuperscript{1}, C\textsubscript{60}\textsuperscript{2}, and C\textsubscript{60}\textsuperscript{3} (Figure 3). This was possible because the mono-disperse nature and molecular size of C\textsubscript{60} results in a very sharp Coulomb staircase that can be observed at room temperature. A physical model based on the molecular orbit structure, the 3-D electrostatic charging energy, and the Fermi-level pinning theory yields good quantitative agreement with experiments. This result not only leads to a better understanding of the C\textsubscript{60} molecular orbital structure and corresponding chemical redox levels, but could also potentially pave the way for realizing reliable multi-level molecular memories. Furthermore, this is the first demonstration that the CMOS circuit system can directly control and sense the redox states of nano-scale molecules.

References


Electrochemical Detection of Protein Interactions by Integrated Neuromorphic CMOS Sensors

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Abstract

Electronic detection for protein microarrays holds high promise for autonomous sensor networks. Electrochemical platforms based on field effect transistors (FET) generally require large Ag/AgCl or Pt reference electrodes to properly set the bias points. Chemoreceptive neuron metal oxide semiconductor (CνMOS) with an extended floating-gate structure provides an integrated approach for protein detection without strict need for analyte reference electrodes. The readout FET biasing is set through the control gate that is capacitively coupled to the extended floating gate. Current-source active biasing can be readily achieved by an internal feedback circuit. With a covalent linking approach, CνMOS can detect the capture of streptavidin by biotinylated BSA in real time with a resolution of approximately 0.025 µg/cm² or 2Å changes in protein layer thickness. Both spectroscopic schemes between 1 kHz and 100 kHz and frequency tuning for high sensitivity can be performed. Through capacitive sensing, this approach eliminates DC charge transfer problems at the sensor interface, which is a common problem for existing electrochemical detection schemes.

Summary of Research

FET sensors have long been used in biosensing [1] and electrochemical detection [2]. Traditionally in the ion-sensitive FET (ISFET) structure, sensing is performed directly on the gate oxide or additional coatings, while a reference electrode such as Ag/AgCl or Pt induces the field effect through the analyte. The detection of protein binding using various tethering schemes has been reported with an ISFET-style sensor in impedance spectroscopy configuration [3]. Such efforts, though successful, prevent utilizing the full potential of CMOS devices in protein microarrays since scaling advantages of CMOS are overshadowed by the need for a relatively large, highly-stable reference electrode, whose presence is often invasive to the analyte for in vivo sensing as well.

Results

An impedance spectroscopic arrangement allows CνMOS (Figure 1) to operate without strictly requiring a reference electrode. CνMOS has fabrication similar to FLASH memory cells. A final passivation oxide etch exposes polysilicon sensing gate to microfluidics. Protein attachment was performed directly on silicon dioxide after treatment with (3-glycidoxypropyl)trimethoxysilane (3-GPS). This attachment scheme provides substantial simplicity over APTS, gold-thiol, biotin/avidin tethering techniques. Biotinylated-BSA was covalently bound to the 3-GPS.

Streptavidin acted as the capture analyte. Models of CνMOS predict increasing drain current with decreasing
sensing gate capacitance [4] (Figure 2). To characterize the films, silicon wafers were used as witness substrates in the covalent attachment procedure and film quality was assessed by an ellipsometer. An AC voltage was provided to the control gate input and to the reference input of a lock-in amplifier. The drain current is transduced to a voltage with a transimpedance amplifier (TIA) and fed to both a lock-in amplifier and oscilloscope for analysis. When the streptavidin binds to the biotinylated BSA, the effective thickness of the protein layer grows and the analyte capacitance decreases, which can be monitored in real-time at a single frequency of high sensitivity surface (Figure 3). The final protein thickness equals 18Å, which corresponds to 69% surface coverage. A calibration curve can be constructed to relate captured protein mass from CvMOS output and control samples monitored by ellipsometer (Figure 4). Protein thickness can be converted to surface coverage of the layer of streptavidin. We can conclude that CvMOS can monitor 0.025µg/cm² or 2Å change in protein layer thickness with a dynamic resolution on the order of 50s.

References

Interdigitated Electrodes for Organic Solar Cells

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Abstract

A new device structure is proposed for organic solar cells, whereby multiple organic semiconducting layers are deposited in between inter-digitated electrodes. It aims to have the multiple advantages of efficient light absorption, and charge carrier generation and collection. Inter-digitated electrodes have been fabricated using a wet-etch undercut method as well as a two-step lithography process. The first yielded small electrode gaps of ~ 200 nm between rough electrodes, while the second produced a gap of ~ 450 nm with much smoother electrodes.

Summary

Organic solar cells have attracted much attention in recent years due to their significant cost advantages and ease of processing and fabrication as compared to their inorganic counterparts (such as silicon cells). A major drawback of organic solar cells is their low efficiency, and a lot of work has gone into getting better efficiencies from these cells.

To achieve high efficiency, it is necessary to incorporate a heterojunction, which is an interface between a donor and an acceptor organic semiconductor material. Excitons created by photon absorption in either material diffuse to the heterojunction, which are then dissociated into electrons and holes due to the offset in the highest occupied molecular orbital/lowest unoccupied molecular orbital (HOMO-LUMO) levels of the two materials. Good light absorption, efficient exciton dissociation and charge carrier collection are all important for a highly efficient cell. The two most common device structures are the bilayer heterojunction and the bulk heterojunction, neither of which boasts all three of the above mentioned properties.

We propose a new "planar" device structure that incorporates all the above features. Such a structure consist of interdigitated electrodes of two metals with different work functions, with multiple donor and acceptor organic semiconducting layers deposited in between. Figure 1 shows a schematic of the cross section of such a device. Individual layers can be made as thin as necessary to facilitate exciton diffusion, while multiple layers can be deposited to increase light absorption. Finally, the charge collection will be driven by the electric field arising from the difference in metal work functions, and the carriers will have a connected pathway to the electrodes.

Two different methods have been employed to fabricate the interdigitated electrodes. In the first method, the first metal is patterned by lithography and dry etching (ion milling), followed by a wet etch undercut step. The second metal is then deposited, and unwanted metal is removed by liftoff.

Figure 1: Schematic of cross section of proposed device structure.
This process is good for producing very narrow gaps (~200 nm), but the electrodes have very rough edges (Figure 2). The second method is simply a two-step lithography process whereby the two electrodes are patterned one after the other by liftoff. Much smoother electrodes are obtained (Figure 3), although the gap is significantly larger (~450 nm). Future work will involve the deposition of organic layers in between the electrodes, as well as solar cell testing and characterization.
Growth Study of Pentacene Thin Films and Transistor Fabrication

CNF Project # 775-99

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Abstract

We report the first-ever investigation in situ and in real-time of the structural evolution of organic small molecule thin films of pentacene during deposition by grazing incidence wide angle x-ray scattering. Small molecule films were deposited in a custom-built vacuum sublimation chamber which was fitted on the D1 beam line. These measurements have provided both in-plane and out-of-plane structural information about the growing polycrystalline films from the moment the growth begins. We report a number of interesting features in these measurements and find that the structure of pentacene films is essentially unaffected by the choice of the dielectric substrate. We also show morphological data from ex situ atomic force microscopy measurements and we measure transistor characteristics for these films.

Summary

A thermal silicon oxide layer was grown on a highly doped silicon wafer. The oxide layer served as the gate insulator, while the highly doped silicon acted as the gate electrode. The substrates were cleaned prior to deposition in an ultrasonic bath with deionized water, dried with filtered nitrogen and given a UV/ozone treatment. The samples were placed inside a custom-made deposition chamber with in situ x-ray scattering capability. A 220° Be window is fitted on the vacuum chamber which was mounted at the D1 station of the Cornell High Energy Synchrotron Source (CHESS). The pentacene was vacuum-sublimed from a Knudsen type cell. The thickness and growth rate were monitored using quartz crystal microbalance (QCM). After deposition, atomic force microscopy (AFM) was conducted ex situ in tapping mode using a DI 3100 Dimension microscope.

In this work, we investigated in situ and in real-time the structural evolution of organic small molecule thin films of pentacene during deposition by grazing incidence wide angle x-ray scattering (GIWAXS) [1, 2]. Pentacene films were grown on silicon oxide (SiO$_2$), Shipley 1805, hydrogen silsesquioxane (HSQ) and polymethyl methacrylate (PMMA). All of the above photoresists were spun onto the SiO$_2$. Analysis of the GIWAXS snapshots shows that the pentacene structure remains unaffected. In situ GIWAXS measurements are shown in Figure 1. Snapshots from an early and late growth stages are presented.

Figure 1: In situ GIWAXS measurements of a pentacene film grown on SiO$_2$ (a), (b) and Shipley 1805 (c), (d) Snapshots at different thickness are presented.
We fabricated top contact organic thin film transistors (OTFTs) with these pentacene films [3]. The top contacts were fabricated by gold evaporation using a shadow mask. The dielectric appears to influence the performance of the OTFTs. Figure 2 presents the current density vs. voltage characteristics of devices grown on SiO$_2$ and Shipley 1805. The hole field effect mobility of pentacene in the case of the plain oxide was 0.6 cm$^2$/Vs. On the other hand, the mobility of devices with Shipley was 0.01 cm$^2$/Vs. Shipley 1805 provided a suitable surface to successfully grow pentacene films that can be used to fabricate OTFTs, but their device performance was inferior to devices using silicon oxide as dielectric. A comparison of the AFMs acquired from films grown on these dielectrics is shown in Figure 3.

References


Direct Measurement of the Electric Field Distribution in a Light-Emitting Electrochemical Cell

CNF Project # 775-99
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Abstract

The interplay between ionic and electronic charge carriers in mixed conductors offers rich physics and unique device potential. One example of such a device is the light-emitting electrochemical cell (LEEC), in which the redistribution of ions assists the injection of electrons and holes from metal electrodes, leading to efficient light emission. We report the fabrication of planar LEECs and probe their operation using electric force microscopy.

We show that obtaining the appropriate boundary conditions is essential for capturing the underlying device physics. To achieve this, we developed a patterning scheme that avoids overlap between the mixed conductor layer and the metal electrodes, allowing an accurate in situ measurement of the electric field distribution inside an LEEC. The measurements show that accumulation and depletion of mobile ions near the electrodes creates high interfacial electric fields which enhance the injection of electronic carriers.

Summary of Research

Electric force microscopy (EFM) allows direct microscopic determination of local potential [1]. The voltage applied to a metal coated cantilever is swept, producing a frequency shift which is parabolic about the local potential. Unfortunately, the sandwich-type configuration which is used in LEECs to minimize the thickness of the iTMC layer is not amenable to facile probing. To enable a direct measurement of the electric field distribution in LEECs with EFM, planar devices were fabricated in which a [Ru(bpy)$_3$]$_2$$(PF_6)_2$ film was spin coated onto an insulating substrate with pre-patterned Au electrodes.

Figure 1 shows the distribution of the potential (A) in these devices. The thin solid trace, which indicates the first measurement after the application of a 5V bias, shows that the potential drops linearly as a function of distance between the two electrodes. The corresponding electric field is approximately constant, indicating that the [Ru(bpy)$_3$]$_2$$(PF_6)_2$ film acts as a resistor. After one hour of continuous application of bias, during which steady-state is reached, the electric field (thick solid trace) shows a small enhancement near the cathode, accompanied by a slight decrease throughout the rest of the [Ru(bpy)$_3$]$_2$$(PF_6)_2$ film.

Based on this electric field distribution it is not possible to unambiguously discriminate between the two models of LEEC operation, and hence it is not possible to pin down the underlying device physics. A closer observation of the data, however, reveals considerable changes of the potential over the anode. This phenomenon can be understood by the diffusion of the PF$_6^-$ counter ions over the metal electrode. This action causes measurements on unpatterned planar devices to fail to capture the relevant device physics of LEECs.

In order to establish the same boundary conditions as in sandwich-type devices, the [Ru(bpy)$_3$]$_2$$(PF_6)_2$ layer needs to be patterned to avoid overlap with the metal electrodes.

Figure 1: In situ potential profile across an unpatterned device.
This was achieved by using a variation of the parylene lift-off technique developed by DeFranco, et al [2]. Parylene is a chemical-vapor deposited polymer which offers conformal, pinhole-free coatings that adhere weakly to a variety of substrates, including freshly cleaned gold [2]. Planar devices were prepared using the process illustrated in Figure 2. In short, gold was deposited on an oxidized silicon wafer. A layer of parylene was then deposited on top and patterned by photolithography and reactive ion etching. An ion mill was used to etch the gold, with the parylene layer acting as an etch mask. A layer of $[\text{Ru(bpy)}_3]^{2+}(PF_6)_2$ was then deposited from solution and patterned by peeling off the parylene with the help of adhesive tape. The advantage of this technique is that the $[\text{Ru(bpy)}_3]^{2+}(PF_6)_2$ film is patterned in a self-aligned manner between the electrodes, having sufficient contact to inject electrons and holes, while never coming into contact with solvents or developers. A wide range of materials can be patterned in this manner, including vapor-deposited thin films.

Figures 3 and 4 show the distribution of the potential and the electric field, respectively, in devices with a $[\text{Ru(bpy)}_3]^{2+}(PF_6)_2$ layer patterned with the technique outlined above. As with the unpatterned devices, the first measurement (thin solid trace), shows that the electric field is approximately constant between the two electrodes. After one hour of continuous application of the 5V bias, however, a large electric field enhancement is visible near the cathode, and a smaller field is located near the anode (thick solid trace). At the same time, the electric field in the bulk of the device is suppressed from 5.4 ± 1.0 kV/cm to 0.9 ± 0.8 kV/cm, a reduction by nearly a factor of 6. A small electric field is also apparent near the anode. A closer inspection shows that the potential over the electrodes is constant, indicating that the patterned samples effectively confine ions between the two electrodes.

The observation of high interfacial fields has important consequences for the design of LEECs. It explains the ability of these devices to function efficiently even when high work function (hence air-stable) cathodes are used. The high energy barrier at the cathode, which would normally prohibit efficient electron injection, is reduced in width by the interfacial electric field. Smaller counter ions can pack near the electrodes with greater density and produce higher electric fields at the electrodes that help inject electrons and holes more efficiently. On the other hand, if too many ions pile up near an electrode, the resulting electric field will be very high, leading to local electrochemical breakdown of the device. Such phenomena are not only important for LEECs, but for all solid state ionic devices. EFM measurements on planar and appropriately patterned devices can help to quantify these effects, understand the underlying physics, and improve the performance of mixed conductor devices.

References


Plasma Wave Terahertz Electronic Devices

CNF Project # 778-99
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Abstract

Terahertz (THz) plasma wave detectors using the high density 2-D electrons in AlGaInN/GaN-based quantum well heterostructure field effect transistors (QW-HFETs) with submicron single gates and multiple gate arrays have been fabricated to achieve high sensitivity, very fast temporal response and precise tunability. We have demonstrated detection of sub-terahertz and terahertz radiation by GaN HFETs in the 0.2 THz-2.5 THz frequency range (much higher than the cutoff frequency of the transistors) with the noise equivalent power (NEP) of $10^{-8}$ W/Hz^{1/2}.

Summary

Potential applications of terahertz (THz) technology in imaging, medicine, biology, space exploration, covert communications, compact radar ranges, industrial controls, THz microscopy, THz tomography, and homeland security require high sensitivity, high speed, portable and tunable THz detectors. Today, the most sensitive detectors such as Golay cells, pyroelectric detectors and bolometers are either very slow, not tunable and/or not portable. New ideas of using plasma resonances of two-dimensional electrons for tunable emission and detection of terahertz radiation have been proposed [1]. The theory in Ref. [1] predicts that such detectors should have a much higher sensitivity than more conventional terahertz detectors. Also, the plasma wave electronics terahertz detectors and detector arrays tunable by DC bias over a wide frequency range will detect not only the intensity but also polarization and direction of a terahertz beam [2].

The objective of this project was to develop novel GaN-based plasma wave electronics terahertz detectors and sources utilizing the high-density 2-D electrons in submicron HFETs. GaN-based HFETs are probably most preferable for fabrication of plasma-wave-based THz devices. The main advantage of such materials comes from the large value of built-in electric field induced by spontaneous polarization. Due to this field, AlGaInN/GaN-based HFETs have an extremely high sheet electron density (over a factor of 10 higher than that in comparable GaAs-based devices). Such high electron density results in a high velocity of plasma waves that allows to dramatically increase the operating frequency and to achieve operation in the THz range of frequencies for much larger sample sizes. In the course of the project, we designed and fabricated devices with different broadband antenna geometries. Figure 1 shows a plasma wave HFET with monolithically integrated coplanar log-periodic antenna.

The typical response of the 150 nm gate length device to sub-THz and THz radiation is shown in Figure 2. Above 70K, only non-resonant detection was observed. At lower temperature, resonant detection was found. Figure 2a and Figure 2b show the response, $\Delta V$, of the transistors to 0.76 THz and 2.5 THz radiation, respectively, as a function of the gate voltage. The resonant detection reveals itself as...
a shoulder or maximum on the monotonic background of the non resonant detection. We attribute this behavior to the resonance detection of THz radiation by plasma waves. One of the most important parameters of the detectors is the Noise Equivalent Power (NEP), which can be found as $N/R_w$, where $N$ is the noise of the transistor in V/Hz$^{0.5}$ and $R_w$ is the responsivity. Figure 3 shows the NEP for different transistors at 4K and at 300K for different frequencies of radiation. Since detection was studied at zero bias, the noise was taken equal to the thermal noise. As seen from the Figure 2, at frequencies $f<0.76$ THz, the NEP is of the order of $10^{-8}$ W/Hz$^{1/2}$ or smaller. This value is slightly higher than for such commercial detectors as Golay cell, pyroelectric detectors and Schottky diodes, having meantime the potential advantage of operation at very high sampling frequency of several tens of gigahertz. At $f = 2.5$ THz, the NEP is higher because of low responsivity at that frequency. The level of sensitivity can be further improved by utilizing multi finger gate arrays in FETs and optimized antenna structures [3].

We also fabricated GaN lateral heterodimensional Schottky diodes (HDSD) formed between 3D metal and 2DEG, and studied their THZ response. The performance of conventional Schottky diodes used for detecting THz radiation is limited by the RC product. The advantage of HDSD is a small junction capacitance, and hence, much higher cutoff frequencies than for a conventional Schottky diode. High concentration of the 2DEG in the channel of the device allows for high forward current (200 mA/mm at 2 V) and relatively low series resistance. Figure 4 shows the response to the 200 GHz radiation. The position of the maximum is determined by the tradeoff between the maximum nonlinearity of the diode and match of the load resistance to the resistance of the diode. As seen, the position of the maximum shifts to lower voltages with the increase of the load resistance. The strongest response was observed when the diode operated in the open circuit configuration. The detection was observed in the frequency range from 200 GHz with the noise equivalent power (NEP) of $10^{-9}$ W/Hz$^{1/2}$ up to 2.24 THz with NEP $\approx 10^{-4}$ W/Hz$^{1/2}$ [4].

References

Fabrication of Sub-22 nm Bistable Devices

CNF Project # 1205-04
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Bistability in 500+GHz sub-22nm quantum dot gate InGaAs-InP FETS for next generation analog and digital circuits for advanced radars and communication systems

This project describes a methodology to design and fabricate digital and RF circuits (requiring lower voltage and significantly reduced device count than conventional CMOS designs) via the use of novel quantum dot gate InGaAs-based 500+ GHz Field-Effect Transistors (FETs), which will exhibit three states in a similar manner to the quantum dot gate Si FETs recently fabricated by our group. Project Sponsor: Office of Naval Research

Information Theoretic Foundation of Molecular Computing

Performance Limits and Design Optimization: This project investigates usage of nanostructure devices for realizing computing systems. The objectives include building molecular logic blocks and memory unit based on quantum dot nanodevices fabricated in our UConn laboratory. Fault tolerant high parallel non-deterministic nanoarchitectures are being investigated. Project Sponsor: National Science Foundation. [With L. Wang.]

A mosaic layout with the integration of FETs and memory devices is being developed to create advanced nano-architecture to implant molecular computing systems.

Bistable Quantum Dot Gate Field-Effect Transistors Exhibiting a Multi-State Operation

A Novel Approach to Reduce Device Count in ICs: This project aims at designing and fabricating Si sub-22nm FETs having 3-state transfer characteristics for multi-valued logic and analog systems. The circuit implications of 3-state devices include lowering number of devices used to achieve a given functionality. Project Supporter: National Science Foundation.

CNF e-beam, RIE and other facilities are being used to implement a design file that will enable fabrication of sub-22nm Si FETs. We are currently working with Daron Westly to show the feasibility of various steps. This work is in progress.

Figure 1: E-beam patterned InP-InGaAs Sample 2A
[January 12th, 2007, Rob Ilic with Ron LaComb]

Figure 2: SiO2 coated InP Sample 1A
[January 12th, Ron LaComb with Rob Ilic]
Fabrication of Si Set Transistors for Electrical Metrology and Ultra-Sensitive Electrometry

CNF Project # 1248-04
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Abstract

This project entails fabrication of silicon (Si) nanotransistors with multiple levels of gates, for two purposes: 1) Silicon single-electron tunneling (SET) devices at low temperatures, and 2) Electrostatic sensing of charge recongurations in fluid at room temperature. We are fabricating these devices on silicon on insulator (SOI) wafers; with back gate, the active layer, two layers of poly-Si gates, and metallization, the process flow has about 60 steps in it. So far, we have made two sets of wafers which have shown promising results, although they are clearly far from optimum.

Summary of Research

Single-electron tunneling (SET) devices, which are based on Coulomb blockade physics, offer the amazing possibility of moving electrons one-by-one. For NIST, these devices offer the potential to form fundamental standards of current, capacitance, or charge [1].

SET devices have been made in a variety of materials, including metal (Al/AIOx/Al), semiconductor (Si and GaAs), nanotubes, granular materials, and etc. Si-based SET devices [2] offer some advantages, including both the potential for higher speed as well as a substantial reduction in the problematic “charge offset drift”. This latter problem refers to the unpredictable random fluctuation in time of the operating point of the device [3], which makes it difficult or impossible to integrate or parallelize these devices. We have shown that, in Si-based SET devices, this fluctuation is reduced by a large factor, of order 1000 [4].

The basic device element for SET devices is a quantum tunneling barrier. In many Si-based SET devices, the tunnel barrier has a fixed value of conductance, set by the material architecture. We have shown that Si-based SET devices in which the tunnel barrier is produced and controlled electro-statically by a “finger” gate (a finFET), the device has better performance and in particular better homogeneity and uniformity [5].

The project at CNF is to fabricate such devices with two levels of gates, lower finger gates and a large upper gate—see Figure 1 for a schematic. Figure 2 shows both a top-
Also, given the leakage problem, we were especially pleased to find that, just as in previous Si-based devices, the charge offset drift problem appears to be quite small in these devices. Figure 4 shows a plot of the charge offset, in units of the electronic charge $e$, measured over many days.

In the coming year, after training a new user, we hope to fabricate multiple sets of wafers in which we have removed the problem of leakage to the back gate; we will then continue our low-temperature SET measurements and assess the performance of the new wafers.

**References**


Ballistic Transport Investigation and the Ballistic Deflection Transistor

CNF Project # 1301-04
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Abstract
In this work, we have been investigating the properties of non-linear ballistic transport and optimizing the design of a novel device, the ballistic deflection transistor (BDT). The electron steering effect required for an operational BDT has been demonstrated. A T-branch junction is also investigated.

Research Summary
The BDT utilizes a novel non-linearity first discovered by Song et. al. [1, 2], and is best understood as a shift in energy created by an artificial scattering mechanism rather than a PN junction. We are currently developing a transistor based upon this non-linearity in combination with electric gates that direct electrons to the appropriate portion of the artificial scatter. The general structure of the device is a cross-shaped structure with a triangular section removed from the intersection of the cross, with two lateral gates on the longer portion of the cross. The removed triangular section acts as the artificial scattering mechanism, and in combination with the gates enable direction of electrons to either lateral channel. A bias current is applied across the long section of the device much in the same way as an electron gun in a CRT, with the gates acting as the steering field. Figure 1 presents a scanning electron micrograph (SEM) of a recently fabricated design.

The fabrication of the device begins with the growth of an InGaAs-InAlAs heterostructure on an InP substrate by molecular beam epitaxy. Gold alignment marks suitable for electron beam lithography are created to enable multiple alignment steps. Hard mask formation is achieved by the evaporation of carbon and a thin layer of SiO$_2$ followed by patterning using PMMA resist. Exposed areas are subjected to a CF$_4$ plasma that removes the SiO$_2$, followed by an oxygen plasma that removes the carbon, creating a transfer mask. The etch is achieved using an ion mill. Lateral gates are formed from the semiconductor and are patterned at the same time as the rest of the structure. The contact layer is then formed using Ni-Ge-Au contacts.

Figure 1: SEM image of a ballistic deflection transistor.

Figure 2: Left and right output voltage response to a push pull voltage.
This structure will have several advantages over conventional transistors. The lateral gates only direct current, and are not used to stop the current through the device (though they can deprive a channel of current). This improves the transit time through the device. The general structure of the transistor is essentially a differential pair rather than a single on/off switch, and this increases the compactness of subsequent circuits. Also there is no intrinsic threshold as such; current is always flowing but is controlled between two ports. The switching voltage is a ratio between the bias voltage and gate size, and as such, very low voltage operation is possible (below 100 mV) with noise being the limiting factor. Recent measurements have demonstrated the steering effect, however gain has yet to be achieved (see Figure 2). We are currently modifying the design to reduce the induced built-in potential of the etched regions near the gates. This built-in potential has been shown to be impeding the steering effect and is the cause of the low gain at this time.

In addition to the transistor structure, we are investigating the fundamental properties of ballistic transport. Here we focus on one such device called the T-branch junction (TBJ) [3]. It has a large nonlinear input-output transfer function on the order of unity. Recent experiments [4] indicate that the intrinsic nonlinearity persists at high frequencies, to at least a terahertz. Therefore the nonlinear current mechanism of the TBJ could in principle be used to build electronic circuitry at unprecedented high frequencies. An SEM picture of one of our TBJs is shown in Figure 3 and typical electrical results are shown in Figure 4. We see that when a push-pull voltage \( \pm V \) is applied, the central probe voltage \( V_C \) is always zero or negative. If the TBJ were ohmic / diffusive, we would expect \( V_C = 0 \) at all \( V \). But to a good approximation, \( V_C \) in Figure 4 can be described as zero for \( V < 200 \text{ mV} \), a straight line with slope near \( \pm 1 \) for larger \( V \), and a gradual transition region between. The \( \pm 1 \) slope implies that \( V_C \) is to some extent pinned to the voltage at which electrons enter the T-bar, from whichever side. Also, the current through the top of the T is proportional to \( V \) (apparently ohmic) until it appears to partially saturate at the same transition region. This correlation between current saturation and onset of negative \( V_C \) is observed with all device geometries and temperatures. This strongly suggests that the two phenomena are caused by the same mechanism.

Our experiments and device structures have demonstrated that non-linear devices can be fabricated using ballistic transport. TBJs exhibit a near unity voltage-in over voltage-out response. The BDT has shown that it is possible to create a steering effect by using lateral fields without depleting the channel; as well it has been shown that the artificial scattering objects can perform as an active load in this device. In the near future, we expect to produce a BDT with gain.

**References**


Fabrication of SOI-Based Nanowire Sensors

CNF Project # 1353-05
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Abstract

Silicon nanowire sensors are fabricated from the active silicon layer of silicon-on-insulator (SOI) wafers and used for label-free sensing of specific proteins. A fabrication method is demonstrated which avoids the integration difficulties inherent in a bottom-up approach, without the decrease in carrier mobility usually associated with reactive-ion-etched nanowires. Nanowire devices are used to demonstrate the label-free detection of below 10 femtomolar concentrations of specific proteins.

Summary

Label-free sensing of specific proteins using semiconductor nanostructures is an important technological breakthrough that has been demonstrated recently, owing to improvements in the ability to fabricate semiconductor nanostructures. However, most if not all of the results published thus far have suffered from low-carrier mobility, resulting in reduced sensitivity, as in the case of most top-down fabricated nanowires, or they have not been easy to integrate into a complementary metal oxide semiconductor (CMOS) process, usually the case for “as-grown” nanowire devices [1-8]. We demonstrate a process to fabricate silicon nanowire metal oxide semiconductor field effect transistors (MOSFETs) with near bulk-mobility and using these devices, demonstrate label-free sensing of proteins.

Using electron-beam lithography with a combination of wet- and dry-etching techniques, we have successfully realized nanowires down to a few tens of nanometers in width on ultra-thin silicon-on-insulator wafers. The resulting nanowires are contacted using optical lithography...
and electrically characterized. Process details are reported in [9]. Figure 1 shows a scanning electron micrograph of the silicon nanowire portion of a typical device. The devices are back-gated using the SOI handle and have a threshold voltage of ~ 20 volts with a sub-threshold slope of ~ 1V. Figure 2 shows a typical drain-current versus gate-voltage characteristic. Field-effect hole-mobility is typically around 100 cm²/V-s for p-channel devices.

Silicon nanowire MOSFETs have been used to demonstrate sensing of a variety of different analytes. Un-functionalized nanowires are used as hydrogen ion sensors to measure pH of a solution, as shown in Figure 2. The steps represent pH values varying from 6.0-8.0. Sensing of specific proteins is also demonstrated using the familiar biotin-streptavidin system, as shown in Figure 3. The device is a p-channel nanowire FET, and streptavidin, a negatively charged molecule, is added at t = 0. Sensitivity below 10 femtomolar concentration is achievable. We are currently applying this new technology to a wide range of chemical and biological systems.

References