Ballistic Deflection Transistor Development

CNF Project # 1301-04
Principal Investigator: Martin Margala

Abstract:

The ballistic deflection transistor utilizes a novel non-linearity first discovered by Song et. al [1,2]. This non-linearity is based upon a shift in momentum created by an artificial scattering mechanism rather than a PN junction. We are currently developing a room temperature transistor based upon this non-linearity in combination with electric gates that direct electrons to the appropriate portion of the artificial scatter. The materials used are InGaAs-InAlAs forming a heterostructure that creates a two dimensional electron gas (2DEG). The general structure of the device is a cross shaped structure with a triangular section removed from the intersection of the cross, with two lateral gates on the longer portion of the cross. The removed triangular section acts as the artificial scattering mechanism, and in combination with the gates enables direction of electrons to either lateral channel. A bias current is applied across the long section of the device much in the same way as an electron gun in a CRT, with the gates acting as the steering field.

Summary:

This structure has several advantages over conventional transistors. The lateral gates only direct current, and are not used to stop the current through the device (though they can deprive a channel of current). This improves the transit time through the device. The lateral gates also integrate the gate noise reducing the noise of the device. The general structure of the device is inherently a differential pair rather than a single on/off switch, increasing compactness. Also there is no intrinsic threshold as such; current is always flowing but is controlled between two ports. The switching voltage is a ratio between the bias voltage and gate size, and therefore, a very low voltage operation is possible (below 100 mV) with noise being the limiting factor.

The fabrication of the device begins with the growth of the heterostructure using molecular beam epitaxy. The InGaAs-InAlAs heterostructure is grown on an InP substrate with the optimization being mean free path at room temperature. Gold alignment marks suitable for electron beam lithography are created to enable multiple alignment steps. Hard mask formation is achieved by the evaporation of carbon followed by patterning using XR-1541 resist. Unexposed areas are subjected to an oxygen plasma that removes the carbon, creating the transfer mask. The etch is achieved using an ion mill. Lateral gates can be formed one of two ways, as a semiconductor or as a metal. For semiconductor gates, they will be patterned at the same time as the rest of the structure. For either type of gates, a layer of XR-1541 is exposed and used as an oxide layer. A contact layer is then formed using Ni-Ge-Au contacts and annealed at 350°C for 30 seconds. If metal gates are required, an additional liftoff process is performed to create the metal gates. Currently, gate formation has been the most challenging portion of this project with only limited success observed.

The recent measured results have shown successful fabrication of the microchannels required for non-linear behavior. This diode type non-linearity is the enhancement by the deflective structure. While triode behavior has been observed at this level (by altering the bias voltage and measuring the output port voltages), we have not achieved gain in this fashion. The gates will enhance this non-linearity to provide gain for this device. The non-linear behavior of the channels is currently being modeled based upon a kinetic inductance and quantum resistance. Initial results indicate an inherent high frequency oscillator transport property that is proportional to electric field strength for narrow 2DEG channels as a possible source for the non-linearity.

References:


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Figure 1: Fabricated ballistic deflection transistor. The top port is referenced as $V_b$, with the left and right ports considered $V_c$ for the measurements shown. The gates are currently non-functional.

Figure 2: IV curves taken from ground to $V_c$, with $V_b$ voltages from top to bottom of -1, -0.5, 0, 0.5, and 1 Volts respectively. Solid lines are measured results, dashed are the mathematical model.

Figure 3: Equivalent circuit used in our mathematical model which assumes a natural oscillation frequency that is a function of electric field.