Development of a Nano-Scale Charge Trapping Memory Array

CNF Project # 804-99
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Abstract:
We have been exploring the use of single/few electrons in distributed storage for use in non-volatile, low power, and fast memories. Providing statistical reproducibility at the nanoscale is a key challenge since we are working with a limited number of storage sites. We have used defects at interfaces of dielectrics (oxide/oxide and oxide/nitride) to evaluate this reproducibility and evaluate the performance of memories. Memory arrays with short channel widths and lengths (30 nm and above) have been fabricated on SOI substrates using electron-beam lithography and the devices and arrays show fast program and erase time. However drain-induced barrier lowering (DIBL) characteristics are degraded compared to large scale devices due to short channel effects (SCE).

Fabrication:
Using a common alignment and mixed-lithography (stepper and e-beam lithography system), 30 nm scale NAND and NOR memory structures and arrays were fabricated. The shortest dimensions—channel width and length—are defined in resist by electron beam lithography combined with pattern transfer through dry plasma processes. Following the active region definition, an SiO₂ spacer is deposited to prevent discontinuity in the very thin and narrow poly-silicon gate which is patterned by e-beam lithography. The electron storage node films, ONO (2.8nm/7.5nm/5nm), are grown and deposited. The nitride and blocking oxide are deposited by LPCVD after bottom tunnel oxide is grown by thermal oxidation. The poly-silicon is deposited immediately following the insulator stack, and this is followed by deposition of oxide that is employed as a hard mask for gate definition using e-beam lithography. A sidewall process with lightly-doped drain and deep implants is employed to obtain suitably electrically scaled structures, and aluminum is employed for interconnects.

Summary:
30 nm dimension 64 bit SONOS with long and narrow gates are fabricated by adding a spacer step after the active processes.

In this experiment, the process for the bulk biasing, which helps prevent floating body effects, has been skipped. Sub-threshold swing of fabricated structures is ~ 250 mV/dec, and the DIBL is a 300 mV/V. These can be improved by reducing ONO layers and increasing channel doping in the next fabrication. Devices where no nitride is employed, defects are grown, and a deposited oxide interfaces are utilized, point to the potential of this approach to scaling the gate stack thickness. In the ONO structures, applying 11 V for 1 µsec causes a 2 V threshold voltage shift from a fully erased condition.

To achieve -2 V threshold voltage shift from a programmed state, -18 V pulse is applied to the gate for 100 µsec. Emission process has a higher activation energy than a capture process due to the use of a cold mechanism. Back tunneling of electrons from the gate has also been observed to cause a slow erase process. Changing fields, such as through the use of high-κ materials instead of ONO layers, can potentially improve the program/erase speed.

References:
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Figure 1, above: Nanoscale SONOS memory arrays of (a) NOR (b) NAND and (c) unit cell.

Figure 2, below left: Characteristics of (a) Programming time and (b) Erasing time.   Figure 3, below: DIBL characteristics.