Organic Electronic Devices and Circuits

CNF Project # 775-99
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Abstract:
Transistors based on organic small molecules and polymers have been studied extensively for more than a decade. In order to realize low-cost circuits for applications such as RFID tags and flexible display backplanes, individual device performance must be optimized by studying material properties and interfaces in the devices, as well as processing techniques used in fabrication. Once these performance parameters are maximized, test circuits must be made to see how they translate into circuit speed and robustness.

Summary:
Organic thin-film transistors can be fabricated using a variety of techniques including inkjet printing, stamping and thermal deposition through a shadow mask. Photolithographic patterning has not received much attention in the organic electronics community partly because the chemicals involved are not compatible with the organic films. Pentacene, the highest performing organic small-molecule, is particularly sensitive to solvents as well as the roughness and chemistry of the surface onto which it is deposited. Photolithography has many advantages over alternative techniques, including high resolution, good registration for multiple level patterning and parallel throughput, which can be scaled to high production capacity, not to mention the 40+ years of industry experience in the technique.

We have demonstrated that the gap can be bridged in many cases using parylene liftoff, a technique invented at Cornell University for patterning cells [1] and adapted for use with organic electronic materials by DeFranco et al [2]. The technique involves depositing and etching a chemically robust polymer (parylene-C) onto the substrate, patterning it with standard photolithography and oxygen plasma etching, and then transferring that pattern to the deposited organic semiconducting material by mechanically peeling the parylene film. Patterns as small as 1 µm have been made with this process. Subtractive patterning can also be accomplished using parylene as an etch mask with similar success.

Using the liftoff technique, transistor electrodes can be made using the conductive polymer PEDOT:PSS with a channel width of 2 µm. Pentacene was used as the semiconducting material in these devices, though it remained unpatterned. A two step process which patterns both the PEDOT and pentacene layers can be found in the second reference.

The next step beyond making individual devices is making simple circuits to test the materials under AC conditions. Though the electrodes in this case are made of metals instead of conducting polymers, the active semiconducting layer (pentacene) is patterned using the same technique used to make the PEDOT:PSS layer in the individual circuits. The pentacene patterning step serves to isolate different circuit elements from one another. Leakage current between the transistors in the ring oscillator would destroy the operation of the circuit by creating shorts.

Optimizing the smoothness of the gate dielectric is vital to the performance of a pentacene transistor, which makes large grains only on smooth surfaces. Larger grains translate to higher mobility because the carriers have fewer grain boundaries to cross. ATEOS (Tetraethyl Orthosilicate) process on the GSI PECVD tool was used to deposit SiO₂ onto the platinum gate electrodes. This produced films with RMS roughness ~ 2 nm, similar to that of the metal electrode.

In conclusion, both individual organic transistors and simple circuits have been fabricated using modified photolithographic techniques, using parylene as a pattern transfer layer.

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Figure 1. PEDOT:PSS electrodes patterned using parylene liftoff technique. Pentacene deposited to form transistor.

Figure 2. Performance of pentacene transistor with PEDOT:PSS electrodes.

Figure 3. A 5-stage ring oscillator. Pt gates and gold electrodes patterned using photoresist liftoff technique on GCA AutoStep. TEOS oxide deposited on GSI PECVD.