Abstract:
Using processes and materials standard to the CMOS industry, this work examines device architectures that can be easily generalized to enable a variety of passive and active planar lightwave circuit (PLC) components such as modulators, switches, resonators, and arrayed waveguides. In this work, 1.55 µm wavelength single mode silicon waveguides are formed from the device layer of a silicon-on-insulator (SOI) wafer, encapsulated in oxide, and then contacts are formed on top of the waveguide using a thin ion-implanted poly-silicon layer. Contacts formed from the top of the device enable two critical benefits: 1) low-loss optical propagation in the crystalline silicon waveguide core and, 2) a common device fabrication process flow for both MOS capacitor and P-I-N diode devices suitable for integration with existing CMOS electronic devices.

Summary:
Rapid development of the field of silicon photonics has been motivated by the need to overcome major challenges in electronic interconnect parasitics. Active silicon electrooptic devices require a careful balance of materials composition, geometry and process flow to create and enable a robust process that leads to practical low-loss, low power, and high speed components. Active components operate by the use of the free carrier plasma dispersion effect (FCPDE) demonstrated in silicon [1].

Single mode 1.55 µm wavelength channel and rib silicon waveguides are formed from the device layer of a silicon-on-insulator (SOI) substrate using e-beam lithography followed by a chlorine-based RIE process (Figure 1). Waveguides are encapsulated in PECVD oxide and the oxide is planarized using chemical mechanical polishing (CMP) to provide a level surface for the formation of the poly-Si contact layer. For MOS capacitor structures a gate oxide is grown and for P-I-N structures, oxide is grown and then removed. Deposited poly-Si then provides a thin, but dense undoped layer, which is subsequently implanted with phosphorous and boron (Figure 2). Some artifacts were observed in the poly-silicon layer geometry and were eliminated through the use of a more conformal oxide deposition process (Figure 3). The waveguides are again encapsulated in oxide to aid in optical coupling [6]. Contacts to the poly-Si layer are formed using sputtered Ti and Al.

While research to date in silicon electrooptics has successfully demonstrated the use of the FCPDE in achieving high-speed optical modulation [2-5], we believe this is the first demonstration of sufficiently general device architecture for integration with CMOS electronics.

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References:
**Active Silicon Planar Lightwave Circuit Elements**

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**Figure 1:** Race-track ring resonators with a coupler gap of 90 nm for enhanced coupling efficiency and a 25 µm circumference for low loss propagation and high Q filtering.

**Figure 2:** Photomicrograph of buried rib waveguide leading into the MOS capacitor region.

**Figure 3:** SEM image of MOS capacitor cross-section. Rib waveguide rests on buried oxide of SOI. Connections to the rib waveguide and the poly-silicon electrode provide electrical bias.

**Figure 4:** Current-voltage characteristics of a typical PIN diode device.