Electrostatically-Gated Nano MOSFETs as Coulomb Blockade Devices

CNF Project # 1248-04

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Abstract:
This project, started about nine months ago, concerns the fabrication of electrostatically-gated nano MOSFETs in Si. The main motivation is to make devices which will act as single-electron tunneling (SET) devices at low temperatures, using the Coulomb blockade, or as electrostatically sensitive nanoscale MOSFETs at room temperature. In particular, we wish to make devices that act as nano-transistors (which are sensitive to the motion of single electrons) and SET turnstiles (which can control the motion of single electrons).

Summary:
There are two main motivations for making these devices:
1) We wish to use the SET turnstiles to provide a fundamental current standard. If we can run one or a large number of these devices at high enough frequencies to provide more than about 100 pA of current, based on the fundamental charge of the electron through \( I = e f \), we can pursue an experiment called “closing the quantum metrology triangle”. This experiment aims to look at the self-consistency between the Josephson voltage standard, quantum Hall resistance standard, and SET current standard.

2) By inverting the Si between heavily-doped source and drain, provide continuous conduction path for the transistor.
2) By depleting selected short regions of the wire, turn those short regions into either tunnel barriers (for SET turnstiles) or sub-threshold regions (for room temperature electrometers).

To date, because this project has just started this year, we have not yet made any functioning devices. We have only finished most of the characterization tests, and are beginning to try to integrate various processes to make partial devices. For that reason, we have no publications to list in the references section.
Objective: Fabricate nano MOSFETs with both lower and upper gates on SOI wafers.

Status: Project started nine months ago; characterization tests finished, integration of different process steps beginning now.

Figure 1, top: Schematic of device architecture.

Figure 2, bottom: Large Si pads with narrow gap etched between them for leakage test.