Bump Bonding Tests for Pixel Array Detectors

CNF Project # 930-01

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Abstract:
Pixel Array Detectors (PAD) for x-ray imaging are being developed that utilize CMOS electronics [1, 2]. These detectors have the potential to exceed the capabilities of traditional CCD detectors and more efficiently use beam time at synchrotron sources.

A PAD consists of two layers: a silicon diode detector layer in which x-rays convert and create electron-hole pairs, and an application-specific integrated circuit readout-chip to process the charge created within the detector layer. Fabrication of a working detector involves electrically coupling each detector pixel with each readout-chip pixel by a process known as bump bonding. Since each detector die typically consists of an array of larger than 100 x 100 pixels on a pitch of 150 µm or less, bump bonding is a challenging engineering hurdle in PAD development.

Our work at the CNF involves fabricating devices which emulate the detector and readout-chip and allow tests of the yield of a vendor’s bump bonding and our collaborator’s in-house flip-chip technique.

Summary:
Wafers were fabricated to test for electrical connections after bump bonding. The techniques used include sputter deposition, conventional contact photolithography, wet-etches, PECVD of passivation layers, and plasma-etching of silicon nitride and silicon oxide. By electrically connecting every other pair of bonding pads on both the readout-chip die and the detector die, the ends of a row show electrical connectivity if every bump successfully connects the detector pad to the readout-chip pad [3]. The use of contact lithography allowed the fabrication of dies larger than the typical stepper die giving us the opportunity to emulate a maximum size CMOS pixel-array while still including easy to probe test pads at the ends of each row. Assuming a high bump yield, this daisy-chain configuration allows quick and easy testing of many bump connections simultaneously.

To date, two vendors have processed the test structures with different techniques for bump bonding. One vendor uses a benzocyclobutene organic passivation before depositing a under bump metallurgy (UBM) upon which solder is electroplated in the gaps of a thick patterned photoresist. After solder electroplating, the photoresist is removed and then the solder is refloved to provide good contact between the solder and UBM. Finally, the field UBM is etched to finish the readout-chip processing. The process flow of the detector wafers is similar to that of the readout-chips with the crucial difference being the replacement of the solder electroplating with the electroplating of a Ni/Au solder-wettable bond pad metallization [4]. A second vendor uses an electroless (and maskless) Ni/Au plating process to deposit the UBM. The plating process is followed by solder ball placement by a dedicated machine that places 5-10 balls a second or by using larger (~30 µm) UBM bumps and joining the two layers with a paste. The electroless processes have not been used as extensively as electroplating processes for PAD hybridization but have the potential to be more cost-friendly.

Initial testing of daisy-chained hybrids is underway. During 2005-2006, we plan to work with vendors to optimize yield and evaluate other bump bonding techniques.

References:
• Pixel-array detectors require bump bonding of the detector chip and integrated circuit readout chip.

• We fabricated wafers for daisy-chained testing.

Figure 1, top right: Micrograph of solder bumps on the bonding pads of the readout chip emulating wafer.

Figure 2, below right: Micrograph of solder-wettable bump capture pads on the detector emulating wafer (Thanks to Alan Huffman from RTI International for figures 1 and 2).

Figure 3, below left: A hybridization of the dies shown in figure 1 and figure 2.