Abstract:
We have demonstrated a new non-volatile storage device that utilizes bipolar injection in a silicon-on-insulator CMOS approach which does not need a control gate and works at relatively high speeds. The structure also provides dense configurability. The principle of the device is based on the injection of electrons and holes through bipolar contacts into the floating gate region to change the state of the device. The writing and erase can be achieved through avalanche processes, channel hot electron injection, and Fowler-Nordheim tunnelling. The avalanche hot electron injection provides fastest programming time of 8 ns with a low program voltage at -13V.

Summary:
Flash memories need to be highly dense and use compatible programming voltages while maintaining low cost. Stacked gate approaches dominate the current flash memory products. However, maintaining scaling in size and voltages is a challenge for these structures. A novel dual-polarity nonvolatile memory cell is demonstrated here to eliminate the erase saturation problem inherent to the F-N (Fowler-Nordheim) erase scheme in the inter-poly dielectrics by eliminating the top control gate. Fast programming/erasing capability has been demonstrated in 1 µm by 1 µm floating gate devices.

Our device consists of a crossed nFET/pFET structure (i.e. a so-called xFET) sharing a common floating gate. Self-aligned source-drain formation was implemented using boron and arsenic implantation at 10 keV and 50 keV respectively for nFET and pFET. The thickness of thermal gate oxide for charge injection is 9 nm. Unlike conventional non-volatile memories, control gate is eliminated in our case to program the device. The cross-coupling structure provides bipolar programmability through charge injection.

By application of a large bias, an avalanche process is created that provides a large flux of carriers (electrons and holes) into the floating gate as in the case of p-channel FAMOS. With the gate connected, this unique memory structure can be operated either as a p-type transistor (pFET) or n-type transistor (nFET), which can be used in combination to provide additional circuit functions. For floating gate device geometries, either set (pFET or nFET) of the device can be used to inject charges (electrons or holes) into the floating gate. The change in conductance of either set can be carefully monitored by using SOI substrate as a back gate (albeit, a lightly doped poor quality gate) to observe sub-threshold transfer characteristics. However, for real application purpose, voltage can be coupled from the nFET contacts to obtain the transfer characteristics of pFET and vice versa. Such threshold voltage change as a function of programming voltage and time are plotted in Figure 2 and Figure 3 to show effective charge injection into the floating gate with programming time down to nanoseconds for electrons on pFET and hundreds of microseconds for holes on nFET.

References:
A Novel Scalable Dual-Polarity-Injection Memory

CNF Project # 804-99

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Figure 1, top right:
SEM image of the device structure.

Figure 2, below left:
Threshold voltage ($V_t$) shift as a function of programming pulse width and pulse voltage applied on pFET.

Figure 3, below right:
Threshold voltage ($V_t$) shift as a function of programming pulse width and pulse voltage applied on nFET.