Abstract:
Monolithic integration of electronics with MEMS elements allows a large variety of applications in areas such as sensors and RF devices for system on chip applications. Process compatibility is a key issue for monolithic integration of MEMS components with CMOS. One of the commonly used processes for MEMS structures release and making micro/nano-fluidic tunnels is removal of sacrificial SiO$_2$ in concentrated HF solution [1]. Wet etch of SiO$_2$ in HF solution is a very reliable process with good selectivity to Si$_3$N$_4$ and very good selectivity to Si.

Common device isolation schemes in standard CMOS processes utilize SiO$_2$ as isolation material, which leads to difficulties in monolithic integration of MEMS and micro/nano-fluidic tunnels which require removal of sacrificial SiO$_2$. Si$_3$N$_4$ is a CMOS compatible HF resistant insulation material, however, Si$_3$N$_4$-Si interface has very high defect and positive fixed charge density which lead to large leakage currents from drain to source and drain to substrate along the sides of the devices [2-4].

Summary:
We have build tri-gate [5] nMOSFETs on bulk silicon substrates using a composite shallow trench isolation (STI) composed of a thin layer of Si$_3$N$_4$, a thicker layer of highly doped polysilicon forming a buried surround side-gate and a thicker layer of Si$_3$N$_4$ as fill material. Cross-sections of the devices resemble a finFET [6] with the exception that the top part of the gate is independently controlled. The devices are defined using optical lithography and the channels are narrowed down by oxidation of the Si active areas and removal of SiO$_2$ formed on the surfaces prior to STI film depositions. The effective widths ($W_{eff}$) of some of the smallest devices are estimated to be as small as 40 nm from the capacitance-voltage measurements performed on the devices. Since the top-gate wraps over the channel of the transistor, the physical channel widths, as viewed from the top, are in the order of 10-20 nm in the smallest devices.

In this device geometry, the top three surfaces of the silicon channel is controlled by the wrapping top-gate just as in the tri-gate or mesa isolated structures build on silicon on insulator (SOI) substrates [5]. In this design, devices are build on bulk Si substrates, hence there is no interface at the bottom of the channel, relieving the problems due to fixed charges at the bottom of the device. Further more this design does not allow the charges to be trapped in the body of the device, hence does not suffer from floating body effects observed in fully depleted SOI devices. The side-gate of the structure surrounds the whole of the active area and it is used to suppress the leakage currents by putting the active-STI interfaces into accumulation of holes as a negative potential is applied to it. This results in excellent device characteristics with leakage currents below 50 fA, subthreshold slopes down to 65 mV/dec. and $I_{on}/I_{off}$ ratios exceeding $10^{10}$ in wide devices.

In the narrow channel devices ($W_{eff} < 200$ nm) the body of the device has very strong coupling to the top-gate on the top portion of the device and to the side-gate at the bottom portion of the device. Application of a large negative bias to the side gate increases the current confinement to the top interfaces, controlled by the top-gate of the device resulting in $I_{on}/I_{off}$ ratios of $10^{10}$ and higher, DIBL less than 5mV/V and no visible threshold voltage roll down to 150 nm gate length. Increased negative side-gate bias is observed to degrade the carrier mobility by approximately 10% for every 1V change in the side-gate bias.

References:
Side-gated tri-gate devices using Si₃N₄ STI.

Negative side-gate bias suppresses leakage currents.

No visible short channel effects down to $L_{\text{eff}} = 150$ nm (no halo implants).

Increased flexibility for MEMS integration with CMOS.

Figure 1, top right: SEM image of a side-gated narrow-channel FET.

Figure 2, below left: Cross section schematics with negative side-gate bias.

Figure 3, below right: Experimental transfer and C-V (inset) characteristics.